Concordia University

Department of Electrical and Computer Engineering

**COEN 212 - DIGITAL SYSTEMS DESIGN I (3.5 Credits)**

**Fall 2019**

"In the event of extraordinary circumstances beyond the University's control, the content and/or evaluation scheme in this course is subject to change".

COEN 212 is taught in three sections. Section D , E and Section F.

Section D

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| Name: | Asim Al-Khalili |
| Room: | EV 5.126 |
| Phone: | (514) 848-2424 ext.3119  |
| E-mail: | asim@ece.concordia .ca |
| Theory: | Tuesdays & Thursdays: 11:45-13:00Room: H531 |
| Office Hours: | Mondays 3:30 pm - 4:30 pm Tuesdays 1:30 pm - 2:30 pm |
| Course Coordinator | Dr. A. Al-Khalili 514-848-2424 x 3119 |

Section F

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| Name: | Dr. Abdul Aziz Trabulsi  |
| Room: | EV 5.209 |
| Phone: | (514) 848-2424 ext 3237 |
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| Theory: | Tuesdays & Thursdays: 11:45-13:00Room: H-407 |
| Office Hours: |  |
| Course Coordinator | Dr. A. Al-Khalili 514-848-2424 x 3119 |

Section G

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| Name: | Bahareh Godarzi |
| Room: | EV 5.245 |
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| Theory: | Tuesdays & Thursdays: 11:45-13:00Room: MB 1.210 |
| Office Hours: | Tuesdays 3:00 — 4:00 |
| Course Coordinator | Dr. A. Al-Khalili 514-848-2424 x 311 |

**Course Description:**

Prerequisite: MATH 204 (Cegep Mathematics 105). Modulo arithmetic: representations of numbers in binary, octal and hexadecimal formats; binary arithmetic. Boolean algebra; theorems and properties, functions, canonical and standard forms. Logic gates and their use in the realization of Boolean algebra statements; logic minimization, multiple output circuits. Designing with MSI and LSI chips, decoders, multi­plexers, adders, multipliers, programmable logic devices. Introduction to sequential circuits; flip-flops. Completely specified sequential machines. Machine equivalence and minimization. Implementation of clock mode sequential circuits. Lectures: three hours per week. Tutorial: two hours per week. Laboratory: 15 hours total.

NOTE: Students who have received credit for COEN 312 may not take this course for credit.

**Course Objectives**

The course aims at giving the fundamental concepts, the design process and the tools that is needed for digital design. Digital circuits nowadays are the building blocks of almost all electronic equipment and gadgets such as computers, communication devices, image processing devices business transactions, military equipment etc. of this digital age. The course covers basic design principals of digital circuits plus popular digital and arithmetic circuit, both combinational and sequential. Up to date digital design flow using high level language and programmable logic devices are also introduced. Analysis of both Combinational circuits as well as Sequential circuits are used to verify the correctness of circuit behaviors. To support the course materials apart from assignments, tutorials are also given on weekly basis plus practical experiments as laboratory work.

**Course Learning Outcomes (CLOs)**

Upon successful completion of the course, students will be able to:

1. Describe the basic design principals of digital circuits and popular digital and arithmetic circuit, both combinational and sequential
2. Describe the use of logic gates in the realization to Boolean algebra statements
3. Specify basic digital circuits using high-level languages and programmable logic
4. Optimize the design parameters of the given problem to meet specific design criteria
5. Derive digital circuit models and solutions to design the final circuits
6. Use tools in their experimental endeavors in the laboratory to proof their concept and correctness of their design. Tools used are: Logic probe and the Digital Design Workstation (i.e. prototyping breadboard) - Model PB503.
7. To understand the limitations of digital circuit design tools in terms of resistance and the capacitance of the measuring equipment and the experimental setups and their effects on power, speed, noise and signal levels.

**Graduate Attributes**

This course emphasizes and develops the following CEAB (Canadian Engineering Accreditation Board) graduate attributes and indicators:

1. A knowledge base for engineering (KB): Demonstrated competence in university level mathematics, natural sciences, engineering fundamentals, and specialized engineering knowledge appropriate to the program.
2. Design (DE): An ability to design solutions for complex, open-ended engineering problems and to design systems, components or processes that meet specified needs with appropriate attention to health and safety risks, applicable standards, and economic, environmental, cultural and societal considerations.
3. Use of engineering tools (UET): An ability to create, select, apply, adapt, and extend appropriate techniques, resources, and modern engineering tools to a range of engineering activities, from simple to complex, with an understanding of the associated limitations.

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| Graduate Attribute | Indicator | Level of knowledge | CLO |
| Knowledge Base | KB-3. Knowledge base in a specific domain (ELEC and COEN) | Intermediate | 1, 2 |
| Design | DE-1. Define the objectiveDE-2. Idea generation and selectionDE-3. Detailed designDE-4. Validation and implementation | Introductory | 3,4,5 |
| Use of engineering tools | ECE-UET-1. Ability to use appropriate tools, techniques, and resourcesECE-UET-3. Demonstrate awareness of limitations of tools, create and extend tools as necessary | Introductory | 6, 7 |

**Course Organization**

TEXT: Digital Design

By Morris Mano, & M. Ciletti, Publisher Pearson, 6th edition [RECOMMENDED and used for assignments and lectures].

LECTURES: (from Digital design by M. Mano and M. Ciletti, 6th edition)

**Chapter 1 & 2**

1. Introduction, Number System, Binary Numbers (2 hrs 30 min).
2. Boolean algebra and Functions (1 hr 15 min).

3. Canonical and Standard Forms (l hr 15 min).

**Chapter 3**

4. K-Map representation (1 hr 15 min).
5. K-Map minimization (1 hr 15 min)
6. 2-level, multilevel representation and minimization (1 hr 15 min).
7. Introduction to HDL (1 hr 15 min)
8. Timing Analysis of combinational circuit (1 hr 15 min)

**Chapter 4**

9. Analysis and design procedures (1 hr 15 min).
10. Popular arithmetic and logical combinational circuits (3 hrs 45 min)
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**Midterm** ( 1hr duration) Total of 11 lectures (Sections: 1.2,1.3,1.4,1.5,1.6,1.7, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 2.9, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 4.2, 4.3, 4.4, Timing Analysis
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11. Decoders/Encoders and MUXes (1 hr 15 min).

**Chapter 5**

12. Introduction to sequential circuits, Latches and Flip Flops (2 .5 hrs.)
13. Analysis of sequential circuits (1 hr 15 min)
14. The state diagram (1 hr 15 min)
15. Synchronous circuit design (3 hrs 45 min.).

**Chapter 6**

16. Registers and counters (2 hrs 30 min.).

**Chapter 7**

17. Memory and PLD (2 hrs 30 min.).
18. Review (1 hr 15 min)

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| **Week** | **Date** | **Chapters covered** | **Topic** | **Events** | **Homework** |
| **1** | Sept.3-9 | 1.1—1.7 | **Number System** |  |  |
| **2** | Sept. 9-16 | 2.1—2.9 | Boolean Algebra | **Tutorials begin** |  |
| **3** | Sept16-23 | 3.1-3.8 | Minimization of Boolean Functions | **Labs begin** | Thursday Sept. 20th |
| **4** | Sept. 23-30 | 4.1-4.4+ timing | Design Process |  | Thursday Sept. 27 |
| **5** | Oct. 1-7 | 4.5-4.10 | Arithmetic Functions,Decoders |  | Thursday Oct. 4th |
| **6** | Oct 7-14 | 4.11 | Multiplexers | **Midterm Exam** |  |
| **7** | Oct 14-21 | 5.1- 5.4 | Latches and Flip Flops |  | Thursday Oct. 18th |
| **8** | Oct-21-28 | 5.5 | Analysis of Sequential Circuits |  |  |
| **9** | Oct28-Nov.4 | 5.7 | Design of Sequential circuits |  |  |
| **10** | Nov. 4-11 | 5.7 | Design of Sequential circuits |  | Thursday Nov. 8th |
| **11** | Nov. 11-18 | 6.1-6.3 | Design of Registers and Counters |  | Thursday Nov. 15 |
| **12** | Nov. 18-25 | 6.4-6.5 | Design of Other counters |  |  |
| 13 | Nov.25- Dec 1 | 7.5-7.8 | PLDs |  | Thursday Nov. 29 |
| 14 | Dec.2-9 | Make-up classes |  |  |  |

TEXT: Digital Design by Morris Mano, & M. Ciletti, Publisher Pearson, 6th edition [RECOMMENDED and used for assignments and lectures.

Lecture contents may be shifted in time depending on time taken to deliver and answering relevant questions.

**LABORATORY:**

There will be approximately 5 experiments. Laboratory classes will start on **(3rd week, the week of Sep. 16th),**

Lab. Coordinator: Tadeusz Obuchowicz, (Ted), SEV5.110, ted@ece.concordia.ca

**Assignments:**

There will be 7 assignments covering the course material.

**Tutorials:** There is a 2 hrs weekly tutorial associated with the lectures that are taken care of by the Teaching Assistants dedicated to the course.

**Evaluation**

Assignments --- 5%

Laboratory-**Passing the lab-work is a requirement.** (15% reports, 5% exam) –20%

Midterm Examination- (Thursday, Oct 10, 2019). -- 25%

Final Exam ---50% (date will be announced later during the course)