**Digital Design COEN 6501 Midterm exam. Oct 17th , 2012**

**Answer all questions. Time allowed 1 hr 30 min.**

**All questions carry equal mark A.J. Al-Khalili.**

**Question-1:**

Using array multipliers give a circuit for calculation of Y:

Y= 2 **N2** + 1

where N is a 4-bit unsigned binary number.

Show this implementation for N=1011. Show the input to each adder clearly. Use “0” when an input is not connected.

**Question-2:**

Design an **8-bit Carry Skip Adder**. Give delay performance of your adder. Show how you calculated your delay at gate level. Calculate area at gate level. Compare this to Carry Ripple Adder of the same

Assume each 2 to 1 MUX is 3 gates. Assume gates of different fan in are equal in delay and area.

**Question-3:**

1. Design a 3 bit shift register. Shifts are from left to right with “0” fill-ins. Start with a state diagram and follow design procedure in each step ending with a diagram.