Department of Electrical and Computer Engineering

COEN 6501 Dec. 9 , 2019

Answer all Questions. All Questions carry equal marks

Exam Duration 3 hour

No books, papers are allowed. Lecturer: Asim J. Al-Khalili

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Question 1

1. What are the advantages of using look up tables in FPGA implementation.
2. Implement **F** using 2:1 MUXs optimally.

**F = AB’ + A’B + AB + ABC**

You are allowed to minimize the function

1. Implement the same functions using look up tables.
2. Compare the results of b) and c) in terms of speed.

Delay of 2 🡒1 MUX is **∆** and the read time of a 2 or 3 bits table is **½ ∆**

**Question2**

Design a shift and add multiplier controller as shown in Fig.1. The controller has two inputs:

 **L**: the least significant bit of the multiplier operand, “0” or”1”

**N**: Counter output “0” or”1”

The controller has one output.  **S**: Stop signal “0” or”1”

Operation of the controller is as follows:

The controller is usually in the idle state.

 If L is ‘1’, then an add and shift operation is performed, If LSB is ‘0’ then a shift operation is performed. In both cases, the counter counts up by one step.

When the counter reaches it desired value N=1, a ***Stop*** signal **S=1** is generated and the state machine goes to the stop state. Design the **sequential circuit *starting with a state diagram***

**Note:** The counter and the reset mechanism are designed separately.

**Shift and Add**

L

N

**S**

 **Fig.1**

**Question 3**

**a.** Identify all the paths in the circuit shown in the Fig. 2 below.

**b.** Determine maximum speed of operation at typical conditions for the

Timing parameters for all components are listed in Table 1.

**c.** If the circuit frequency is 100 MHz, determine the slack time for the setup time and hold time at the D-input of **Flip-Flop D3**

F

**G1**

**G2**

D3

D1

D2

A

B

G3

G4

I1

 G5

CLK

 **Fig. 2**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Component | Tp (ns) | Input Loading (UL) | K1**ns/UL** | K2 ns/fanout |
| Inverter | 0.15 | 1 | 0.05 | 0.1 |
| NAND AND | 0.25 **0.5** | 1.5 **2.0** | 0.1 **0.15** | 0.15 **0.2** |
| OR EXOR | 0.75 **1.0** | 2.5 **3** | 0.20.25 | 0.25 **0.3** |
| Flip Flop, ↑, (CK to Q) **tsu=1 ns, th = 0.5ns** , **tcs= 0.25ns** | 1.5 | 3.5 | 0.3 | 0.35 |

 **Table 1**

**Question 4**

Design a hardware using Booth algorithm to implement A\*B

 **A= - 6 , B= 20**

You may use the following model as a Booth decoder

**Ej = –2Bi + Bi-1 + Bi-2**

Give full circuit diagram and calculate delay of the circuit in terms of full adder delay **ta** and any gate delay **tg**.

**Question 5**

For the circuit shown in Fig. 3 below,

1. Write a structural VHDL code for the entity “Circuit”.
2. Write a behavioral VHDL code, “Test\_Bench” for testing the circuit

Test\_Bench

Circuit

Generator

**F**

**A**

**B**

 **Fig. 3**

1. Draw a response to the following VHDL Code

 ***process***

 ***begin***

 **B<= *not* A ;**

 ***wait until* A=‘1’ *for* 10 ns;**

 ***end process*;**

 A

 10 20 30 40 50 60

 B -------------------------------------------------------------?

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Question 6

Design the **fastest** hardware to do the following operation.
**F = N3 + 1
N** is an unsigned **2-bit** binary number **N= n1 n0.** Evaluate your design in terms of speed

**You may use any method you choose to give the fastest performance.**

**Assume gate delay is tg.**

**Appendix A**

**1. tcs,max < tCQmin + tCLmin + tsu.min**

**2. Tmin ≥ tCQmax + tCLmax+ tsUmaxR2 –tcsmin**

**3. thmaxR2 < tCQmin + tCLmin - tcsmax**

**tCL = tLogic + tinterconnec**