## CDA 3200 Digital Systems

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## Outline

- A Sequential Parity Checker
- "01" Detector
- Analysis by Signal Tracing and Timing Charts


## A Sequential Parity Checker (1/13)

- Parity bit is used to detect errors.
- Example:
- 7 data bits
parity bits
- 0000000

0

- 0000001

1

- 0110110 0
- 1010101

1

- 0111000

1

## A Sequential Parity Checker (2/13)

- Parity checker
- A group of bits is applied to $X$
- Z indicates the parity.



## A Sequential Parity Checker (3/13)

- Goals
- Decide how many flip-flops (FFs) are needed
- Decide the expressions for flip-flop (FF) inputs
- Decide the expression for the final output
- Tools
- Time waveform
- State graph
- State table


## A Sequential Parity Checker (4/13)

- Time waveform
- Can help us understand the problem.
- But cannot help in developing logic expressions.



## A Sequential Parity Checker (5/13)

- State graph
- States are independent of circuit realization.
- They reflect what've happened and maybe also indicate the output.


State zero, where the output is zero.

## A Sequential Parity Checker (6/13)

- In a parity checker, only two states are needed.
- $\mathrm{S}_{0}$ : even number of 1's have been received.
$-S_{1}$ : odd number of 1 's have been received.


All possible transitions have been considered.

## A Sequential Parity Checker (7/13)

- State table
- Can be realization-free.

| Present <br> State | Next State |  | Present <br> Output (Z) |
| :---: | :---: | :---: | :---: |
| $\mathrm{S}_{0}$ | $\mathrm{~S}_{0}$ | $\mathrm{~S}_{1}$ | 0 |
| $\mathrm{~S}_{1}$ | $\mathrm{~S}_{1}$ | $\mathrm{~S}_{0}$ | 1 |

## A Sequential Parity Checker (8/13)

- State table (cont)
- Two states can be represented by 1 bit.

| Present | Next State |  | Present <br> Output (Z) |
| :---: | :---: | :---: | :---: |
| State | $\mathrm{X}=0$ | $x=1$ |  |
| $\mathrm{S}_{0} 0$ | $\mathrm{S}_{0} 0$ | $\mathrm{S}_{1} 1$ | 0 |
| $\mathrm{S}_{1} 1$ | $\mathrm{S}_{1} 1$ | $\mathrm{S}_{0} 0$ | 1 |

## A Sequential Parity Checker (9/13)

- State table (cont)
- Say we are using a T flip-flop (FF) $\left(\mathrm{Q}^{+}=\mathrm{Q}\right.$ xor T$)$

| Present <br> State Q | Next State <br> $\mathrm{X}=0$ |  | $\mathrm{Q}^{+}$ <br> $\mathrm{X}=1$ |
| :---: | :---: | :---: | :---: |
| 0 | $\mathrm{~T}=0$ | 0 | 1 |

How can we decide T's?

## A Sequential Parity Checker (10/13)

- State table (cont)
- Say we are using a T flip-flop (FF) $\left(\mathrm{Q}^{+}=\mathrm{Q}\right.$ xor T$)$

| Q | $\mathrm{X}=0$ | $\mathrm{Q}=1$ | Present <br> Output (Z) |
| :---: | :---: | :---: | :---: |
| 0 | $0 / 0$ | $1 / 1$ | 0 |
| 1 | $1 / 0$ | $0 / 1$ | 1 |

## A Sequential Parity Checker (11/13)

- State table (cont)
- What is the expression for $T$ ? $T=X$

| Q | $\mathrm{X}=0$ | $\mathrm{Q}^{+} / \mathrm{T}=1$ | Present <br> Output (Z) |
| :---: | :---: | :---: | :---: |
| 0 | $0 / 0$ | $1 / 1$ | 0 |
| 1 | $1 / 0$ | $0 / 1$ | 1 |

## A Sequential Parity Checker (12/13)

- State table (cont)
- What is the expression for $Z$ ?
$Z=Q$

| Q | $\mathrm{X}=0$ | $\mathrm{X}=1$ | $\begin{array}{l}\text { Present } \\ \text { Output (Z) }\end{array}$ |
| :---: | :---: | :---: | :---: |
| 0 | $0 / 0$ | $1 / 1$ | 0 |
| 1 | $1 / 0$ | $0 / 1$ | 1 |

## A Sequential Parity Checker (13/13)

- Parity check



## "01" Detector (1/10)

- Detects bit pattern "01" in a serial input
- Input:

0111110100

- Output: 0100000100


## "01" Detector (2/10)

- State graph
- We do not necessarily know how many states are needed ahead of time.
- We can assume an initial state which is before any input.
- Then there will be two transitions from the initial state and they are triggered by 0 and 1.
- A transition may introduce a new state.


## "01" Detector (3/10)



## "01" Detector (4/10)

- $\mathrm{S}_{0}$ : nothing has been received to make a "01".
- $S_{1}$ : "0" has been received.
- S2: "01" has been received.

How many bits are needed to represent $S_{0-2}$ ?

## "01" Detector (5/10)

- State table

| Present <br> State | Next State |  | Present <br> Output (Z) |
| :---: | :---: | :---: | :---: |
| $\mathrm{S}_{0}$ | $\mathrm{~S}_{1}$ | $\mathrm{~S}_{0}$ | 0 |
| $\mathrm{~S}_{1}$ | $\mathrm{~S}_{1}$ | $\mathrm{~S}_{2}$ | 0 |
| $\mathrm{~S}_{2}$ | $\mathrm{~S}_{1}$ | $\mathrm{~S}_{0}$ | 1 |

## "01" Detector (6/10)

- State table (cont)
- Encode states
$-\mathrm{S}_{0}: 00$
$-S_{1}: 01$
$-\mathrm{S}_{2}: 10$


## "01" Detector (7/10)

- State table (cont)
 Present State

Next State $\mathrm{Q}_{1}{ }^{+} \mathrm{Q}_{0}{ }^{+} \mid$Present
$\mathrm{S}_{0} 00$
$S_{1} 01$
$\mathrm{S}_{2} 10$
$S_{1} 01$

| $S_{0} 00 \quad 1$ |
| :--- | :--- |

## "01" Detector (8/10)

- State table (cont): T flip-flops (FFs) are used

| $\mathrm{Q}_{1} \mathrm{Q}_{0}$ | $\mathrm{X}=0$ | $\mathrm{Q}_{1}{ }^{+} \mathrm{Q}_{0}^{+} /$IT $\mathrm{T}_{1} \mathrm{~T}_{0}$ <br> $\mathrm{X}=1$ | Present <br> Output (Z) |
| :---: | :---: | :---: | :---: |
| 00 | $01 / 01$ | $00 / 00$ | 0 |
| 01 | $01 / 00$ | $10 / 11$ | 0 |

## "01" Detector (9/10)

- What are the expressions for $T_{1}, T_{0}, \& Z$ ?

| $\mathrm{Q}_{1} \mathrm{Q}_{0}$ | $\mathrm{X}=0$ | $\mathrm{Q}_{1}^{+} \mathrm{Q}_{0}^{+} /$T $\mathrm{T}_{1} \mathrm{~T}_{0}$ <br> $\mathrm{X}=1$ | Present <br> Output (Z) |
| :---: | :---: | :---: | :---: |
| 00 | $01 / 01$ | $00 / 00$ | 0 |
| 01 | $01 / 00$ | $10 / 11$ | 0 |

## "01" Detector (10/10)

- $\mathrm{Q}_{1} \mathrm{Q}_{0} \times \mathrm{T}_{1} \mathrm{~T}_{0} \quad \mathrm{Z}$
- 000000010
- 00010000
- $0 \quad 1 \quad 0 \quad 0 \quad 0 \quad 0$
- $0 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 0$
- 10000111
- $1 \begin{array}{llllll}1 & 0 & 1 & 1 & 0 & 1\end{array}$
- $1100 \times \times$
- $1111 \begin{array}{llll}1 & 1\end{array}$

Minterms $\rightarrow$ expressions!!

## Analysis by Signal Tracing and Timing Charts (1/6)

- Moore machine
- The output depends only on the present state of the flip-flops (FFs).
$-Z=F\left(Q_{n}, Q_{n-1}, \ldots, Q_{1}, Q_{0}\right)$
- Mealy machine
- The output depends not only on the present state, but also the value of the circuit inputs.
$-\mathrm{Z}=\mathrm{F}\left(\mathrm{Q}_{\mathrm{n}}, \mathrm{Q}_{\mathrm{n}-1}, \ldots, \mathrm{Q}_{1}, \mathrm{Q}_{0}, \mathrm{X}_{\mathrm{m}}, \mathrm{X}_{\mathrm{m}-1}, \ldots, \mathrm{X}_{1}, \mathrm{X}_{0}\right)$


## Analysis by Signal Tracing and Timing Charts (2/6)

- Because flip-flops (FFs) only respond to input at rising/falling edges, the output of a Moore machine only changes at rising/falling edges.



## Analysis by Signal Tracing and Timing Charts (3/6)



## Analysis by Signal Tracing and Timing Charts (4/6)

- In a Mealy machine, outputs changes when flip-flops (FFs) and/or circuit input change.
- Therefore, when the circuit output changes is independent of rising/falling edges.


> Analysis by
> Signal Tracing and Timing
> Charts (5/6)


## Analysis by Signal Tracing and Timing Charts (6/6)

- In a Mealy machine, the output is read immediately before the rising/falling edge.


