## CDA 3200 Digital Systems

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## Outline

- SR Latch
- D Latch
- Edge-Triggered D Flip-Flop (FF)
- S-R Flip-Flop (FF)
- J-K Flip-Flop (FF)
- T Flip-Flop (FF)
- Flip-Flops (FFs) with Additional Inputs


## SR Latch (1/17)

- Combinational circuits
- Outputs depend on present inputs
- Sequential circuits
- Outputs depend on both present and the past sequence of inputs.
- Have memory.


## SR Latch (2/17)



## SR Latch (3/17)



| $X$ | $Y$ | NOR |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

The circuit can assume an initial and stable state: SR/PQ=00/10.

## SR Latch (4/17)



| $X$ | $Y$ | NOR |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

- $\mathrm{SR} / \mathrm{PQ}=10 / 01$ is also stable.


## SR Latch (5/17)



| $X$ | $Y$ | NOR |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

- $\mathrm{SR} / \mathrm{PQ}=00 / 01$ is also stable.


## SR Latch (6/17)



| $X$ | $Y$ | NOR |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

- $\mathrm{SR} / \mathrm{PQ}=01 / 10$ is also stable.
- $\mathrm{SR} / \mathrm{PQ}=00 / 10$ is also stable.


## SR Latch (7/17)



| $X$ | $Y$ | NOR |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

## SR Latch (8/17)



| $X$ | $Y$ | NOR |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

## SR Latch (9/17)



The change between any two of 00,10, 01 will reach a stable state.

## SR Latch (10/17)



| $X$ | $Y$ | NOR |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

-What is PQ
when the circuit is stable?

## SR Latch (11/17)

- $\mathrm{SR}=11$ is restricted in SR latch.
- PQ cannot be both 1 .


## SR Latch (12/17)

- When $\mathrm{SR}=10, \mathrm{PQ}=01$ is stable.
- When $\mathrm{SR}=01, \mathrm{PQ}=10$ is stable.
- When $S R=00$, both $P Q=10$ and $P Q=01$ are stable.
- Note
- In the stable states, $\mathrm{P}=\mathrm{Q}^{\prime}$
- Any change to $S R=00$ will not change $P Q$.
- SR=00 is used to keep states (remember what happened.)


## SR Latch (13/17)


(a)

(b)

S: Set Q<br>R: Reset Q

## SR Latch (14/17)

- How to draw a truth table for an SR latch?
- Input?
- Output?


## SR Latch (15/17)

- S R

Q


- 00
- 01


1

- 01
- 10

1
0
1
1

- 11
$0 \times$
-1 $1 \begin{array}{llll}1 & 1 & X\end{array}$


## SR Latch (16/17)

- Alternatively, an SR latch can be realized using NAND gates.

(a)

(b)


## SR Latch (17/17)

- Alternatively, an SR latch can be realized using NAND gates.

| - S-bar | R-bar | Q | $Q^{+}$ |
| :--- | :--- | :--- | :--- |
| -1 | 1 | 0 | 0 |
| -1 | 1 | 1 | 1 |
| -1 | 0 | 0 | 0 |
| -1 | 0 | 1 | 0 |
| -0 | 1 | 0 | 1 |
| -0 | 1 | 1 | 1 |
| -0 | 0 | 0 | $X$ |
| -0 | 0 | 1 | $X$ |

## Gated D Latch (1/3)


(a)

(b)

- What are $S$ and $R$ when $G=0$ ?
- $\mathrm{G}=0$ keeps states: $\mathrm{Q}^{+}=\mathrm{D}$.
- Can SR=11 ever occur?
- $\mathrm{Q}^{+}=\mathrm{D}$ when $\mathrm{G}=1$.


## Gated D Latch (2/3)



- No "do not care" terms.


## Gated D Latch (3/3)

- if(G==1)\{
- $\mathrm{Q}^{+}=\mathrm{D}$;
- \}else\{
- $\mathrm{Q}^{+}=\mathrm{Q}$
- \}


## Edge-Triggered D Flip-Flop (FF) (1/3)

- If the $G$ signal in the $D$ latch is connected to a clock input, the output changes only in response to the clock, not to a change in D.
- And we call this latch a D Flip-Flop (FF).


$$
\mathrm{Q}^{+}=\mathrm{D}
$$

(a) Rising-edge trigger
(b) Falling-edge trigger

## Edge-Triggered D Flip-Flop (FF) (2/3)


(a) Construction from two gated D latches

(b) Time analysis

## Edge-Triggered D Flip-Flop (FF) (3/3)

Note Q does not change during $\mathrm{Ck}=0$.

-Timing for D Flip-Flops
(FF) (Falling-Edge Trigger)

$$
\text { S-R Flip-Flop (FF) }(1 / 3)
$$

- $\mathrm{Q}^{+}$changes in response to the clock signal.



## S-R Flip-Flop (FF) (2/3)


(a) Implementation with two latches


- When CLK=0
- $\mathrm{P}^{+}=\mathrm{S}_{1}+\mathrm{R}_{1}{ }^{\prime} \mathrm{P}$
- When CLK=1
- $\mathrm{Q}^{+}=\mathrm{P}$
S-R Flip-Flop (FF) (3/3)
- Why master-slave Flip-Flops (FFs)?
- The master Flip-Flop (FF) holds the output for in the first half clock cycle.
- When the slave Flip-Flop (FF) updates and outputs, the master is closed.
- This mechanism guarantees that the final output changes only once in a clock cycle.


## JK Flip-Flop (FF) (1/2)

- An extended version of the SR Flip-Flop (FF)
- J corresponds to S
- K corresponds to R

| -- K Q <br> - 0 0 0 <br> - 0 0 1 <br> - 0 1 0 <br> - 1 0 1 <br> - 1 0 0 <br> - 1 1 0 <br> - 1 1 1${ }^{+}$ | 1 | 1 |
| :--- | :--- | :--- | :--- |

JK can be 11. This
configuration changes the state of Q .

## JK Flip-Flop (FF) (2/2)



- $\mathrm{S} 1=\mathrm{J}$ * $\mathrm{Q}^{\prime}$ * CLK ${ }^{\prime}$
- R1=K * Q * CLK'
- S1 and R1 cannot be 1 at the same time.


## T Flip-Flop (FF) (1/2)

- $\mathrm{T}=0 \rightarrow$ no state change
- T=1 $\rightarrow$ state changes

$\begin{array}{lll}\text { T Q } & \text { Q }^{+} \\ 0 & 0 & 0\end{array}$
$011 \quad Q^{+}=\mathrm{T}$ xor Q
101
110
(a)


## T Flip-Flop (FF) (2/2)


(a) Conversion of J-K to $T$
(b) Conversion of $D$ to $T$

## Summary (1/8)

- All the Flip-Flops (FFs) and D latch are based on SR latch.
- SR latch can be described using
$-Q^{+}=S+R^{\prime}$ Q
- $\mathrm{S}=1$ sets Q
- R=1 resets Q
- $S R=00$ keeps states ( $Q$ does not change.)


## Summary (2/8) $\mathrm{Q}^{+}=\mathrm{S}+\mathrm{R}^{\prime} \mathrm{Q}$

- Gated D latch
$-S=D G$
$-R=D ' G$
- When $G=0, S R==00 \rightarrow$ state kept.
- When $G=1, Q=D$
- When $\mathrm{D}=0, \mathrm{SR}=01 \rightarrow$ reset $\mathrm{Q} \rightarrow \mathrm{Q}=0$
- When $\mathrm{D}=1, \mathrm{SR}=10 \rightarrow$ set $\mathrm{Q} \rightarrow \mathrm{Q}=1$


## Summary (3/8) $\mathrm{Q}^{+}=\mathrm{S}+\mathrm{R}^{\prime} \mathrm{Q}$

- When G is a clock signal, two gated D latches comprise an edge-triggered D Flip-Flop (FF)

if(CLK is low) Q does not change
else
Q becomes D shortly after the rising edge


## Summary (4/8) $\mathrm{Q}^{+}=\mathrm{S}+\mathrm{R}^{\prime} \mathrm{Q}$

- SR Flip-Flop (FF)
- Master and slave
- When the master receives the input and updates, the slave is close.
- When the slave outputs, the master does not respond to any input change.



## Summary (5/8) $\mathrm{Q}^{+}=\mathrm{S}+\mathrm{R}^{\prime} \mathrm{Q}$

- SR Flip-Flop (FF) (cont)
- When CLK is low,
- $\mathrm{S}_{1} \mathrm{R}_{1}=\mathrm{SR} \rightarrow \mathrm{P}^{+}=\mathrm{S}+\mathrm{R}^{\prime} \mathrm{P}$, master is updated
- $\mathrm{S}_{2} \mathrm{R}_{2}=00 \rightarrow \mathrm{Q}$ does not change



## Summary (6/8) $\mathrm{Q}^{+}=\mathrm{S}+\mathrm{R}^{\prime} \mathrm{Q}$

- SR Flip-Flop (FF) (cont)
- When CLK is high,
- $\mathrm{S}_{1} \mathrm{R}_{1}=00 \rightarrow \mathrm{P}$ does not change
- master does not respond to inputs
- $\mathrm{S}_{2} \mathrm{R}_{2}=\mathrm{PP}^{\prime} \rightarrow \mathrm{Q}^{+}=\mathrm{P}+\left(\mathrm{P}^{\prime}\right)^{\prime} \mathrm{Q}=\mathrm{P}$



## Summary (7/8) $\mathrm{Q}^{+}=\mathrm{S}+\mathrm{R}^{\prime} \mathrm{Q}$

- SR Flip-Flop (FF) (cont)

- The final output, Q, was not affected by 01 .


## Summary (8/8) $\mathrm{Q}^{+}=\mathrm{S}+\mathrm{R}^{\prime} \mathrm{Q}$

- JK Flip-Flop (FF)
- Very similar to SR master-slave Flip-Flop (FF)
- Except JK=11 inverts the output
- T Flip-Flop (FF)
$-\mathrm{T}=1 \rightarrow$ inverts the output
$-\mathrm{T}=0 \rightarrow$ keeps the same output


## Flip-Flops (FFs) with Additional Inputs (1/3)

- Clear and Preset signals are two asynchronous signals and do not depend on CLK.

(a)


## Flip-Flops (FFs) with Additional Inputs (2/3)



## Flip-Flops (FFs) with Additional Inputs (3/3)

- Clock enable signal

(a) Gating the clock

(b) D-CE symbol

(c) Implementation

