

ERC32 Evaluators Workshop

Estec 28 January 1998

Fernand Quartier

Agenda (1)

- Introduction
- Product evolution
 - Corrections & speed improvement Target Simulator
 - Corrections Hard Real-time tools
 - Added features Target Simulator
 - GNU Debug integration
 - SHAM integration
 - Revised user manuals
 - Revalidation, publishing and maintenance of SIS
 - Monitor development
 - DSP Simulator
- Planning

Introduction (1)

- Spacebel Overall Technology Approach

- New section: QuoVadis

- Increased need for efficient validation and characterisation tools
 - > Quality Of service Validation, Assessment, Development and Integration Systems
 - ERC32 tools in marketing phase
 - GNU integration, evolution and maintenance
 - Target Simulator for redundant and fault-tolerant systems
 - other segments and derivatives planned (DSP 21020, PowerPC, HRT for multi-CPU)

- High performance parallel systems: ASAP

- Scalable systems (SCASAP)
 - Real-time and parallel/distributed oriented

- CORBA software backplane

Introduction (2)

- Maintain distinctive features Target Simulator
 - Timing accuracy, validated
 - Non-intrusive markers (breakpoints, watchpoints, etc...)
 - Open to scripts, other simulators through IO simulation, OS emulation
 - Flexible stand-alone mode
 - Advanced markers, conditions
 - Powerful scripting (automatic testing, validation)
 - Support

Corrections Target Simulator

- Float format for output
- PROM access protection (problems with half words)
- Updated version of loader
 - Multi-segment S-Record files
 - support virtual and physical address in ELF format
- Improved installation procedure

Speed improvement Target Simulator

- Integrate fast simulation methods from SIS
- No penalty for IO-Environment interface
- Dynamic selection of mode for slower components:
Accurate/Fast
 - UART
 - Access protection
 - Fetching

Corrections Hard Real-time tools

- Fixes & Refinements
 - Convergence in margin analysis
 - Computation time accuracy
 - Change priority assignment (TBC)

Added features Target Simulator

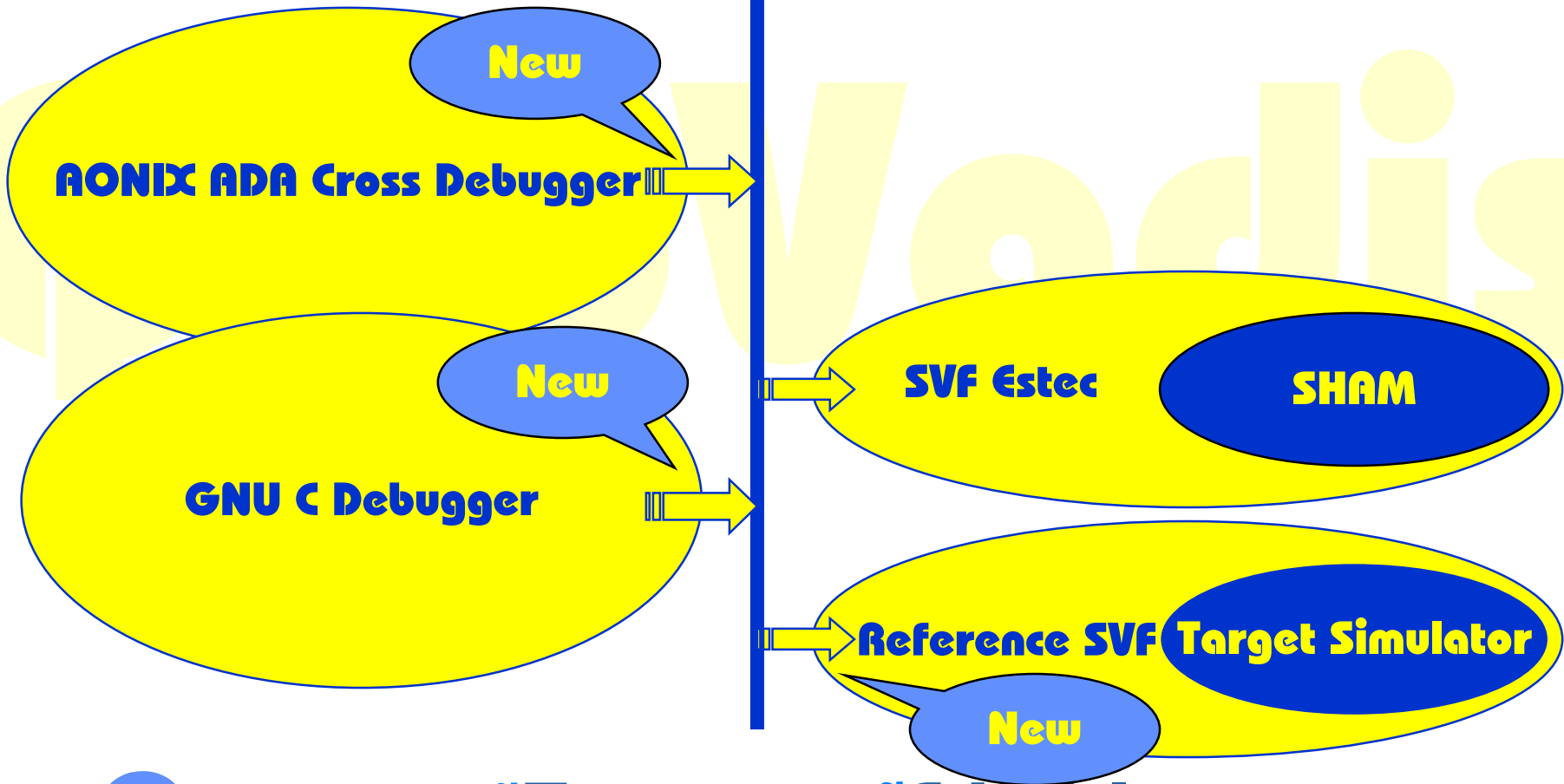
- Coverage bits for memory accesses allows to detect
 - executed /non-executed code
 - reading of variables before writing
 - non used variables
 - self modifying code
 - mixed byte/word addressed variables (to be discussed)

GNU Debug integration

- GNU gdb control
 - non-intrusive
 - no monitor needed
- Merging of Stand-alone mode with gdb
 - powerful scripting
 - access to all commands

SHAM Integration (under negotiation)

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Revised user manuals

- Will be completely revised when all new functionality and interfaces are defined (TS & HRT)

Revalidation, publishing and maintenance of SIS

- Under negotiation
- Revalidation and correction (or documenting) all SIS timing
- Restore the correct UART timing possibility
- New version will be published
- Maintenance support will be offered

Monitor development

- Under investigation
- Should provide transparent access (including Tcl support) to
 - Target Simulator
 - Target and its monitor
- Has to solve the watchdog problem
- Could use part of the MEC memory protection scheme for hardware assisted trace point and trapping

DSP Simulator

- Under investigation
- Identical development chain and tools for "spacialised" 21020 DSP
- Improved visibility on compact 32 bit systems

Planning

- Early 2Q98:
 - Corrections & speed improvement Target Simulator
 - Corrections Hard Real-time tools
- Early 3Q98:
 - GNU Debug integration & added features Target Simulator
- 3Q98:
 - Revised user manuals
- 4Q98:
 - SHAM integration
- TBD:
 - Revalidation, publishing and maintenance of SIS
 - Monitor development
 - DSP Simulator