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Lab 9: Dynamic D Flip-Flops

Objectives

The objective of this lab is to introduce the student to dynamic storage elements. This lab is actually the first part of the VLSI class project.

Dynamic D Flip-Flops

For this lab, you need to set up the circuit in Hspice for a Negative edge triggered Dynamic D flip-flop and verify its functionality. After verifying the functionality of the D flip-flop you need to implement an asynchronous Reset feature to the Negative edge triggered Dynamic D flip-flop and verify the Reset operation as outlined below. Once this has been done, create a schematic for the D flip-flop with the Reset feature added. Create this new schematic in a new library 'lab9'. Note that you should use minimum number of transistors to implement the Reset. Also you must add an inverter stage to produce the uncomplemented output (Q).

Verifying the operation of the D flip-flop

- Create the circuit for your D FF and simulate in Hspice to verify its operation (transistor sizing is up to you). Do this by connecting the FF in a divide-by-two configuration (the 'Q_not' output is tied back to the D input, the Q output will now be the CLK frequency divided by 2).
- Modify the schematic to add a LOW TRUE reset pin called 'R'. This should be an ASYNCHRONOUS reset. Test your new implementation with the following test cases.
 1. Initialize the FF to a '1' (D = '1', R = '1', apply one clock period), then set D = 0, pulse 'R' low (bring to '0' then back to '1') when CLK = HIGH, observe Q going low BEFORE the clock goes back LOW (set the length of the clock period to whatever you want). You should observe Q remaining low for ALL remaining clocks (clock at least a couple of times).
 2. Same as previous simulation except apply 'R' when CLK = LOW.
 3. Initialize the FF to a '1' (D='1', R='1', apply one clock period), then set D=1, pulse 'R' low (bring to '0' then back to '1') when clock = LOW, observe Q going low BEFORE the clock goes back HIGH (set the length of the clock period to whatever you want). You should observe Q remaining low until the NEXT active clock edge, at which point Q should go back high (clock at least a couple of times).
 4. Same as previous simulation except apply R when CLK = HIGH.

This should cover all asynchronous reset cases. Your asynchronous reset SHOULD NOT dissipate static power. Create a plot of supply current ; given a significantly long enough settling period the supply current should always return to near 0. Show that this is the case for you circuit in all of the simulations discussed above when 'R' is asserted.

HSPICE tips

In all tests, you will need to add a capacitor on the output node; use a 15 fF capacitor. Use 50ps (.05ns) rise/fall times for all signals. Use $V_{cc} = 3.3$ volts. Use a long clock period to allow internal node voltages to settle (20 ns should be plenty, you can use longer period if desired). In this lab, we are only worried about functional operation.

When adding the low true reset, you will need to carefully track the states of internal node voltages; you may have to reset more than one internal node voltage. This means adding more than 1 pullup/pulldown transistor. The node voltages you need to be concerned with are those between each stage (between 1st/2nd stages, between 2nd/3rd stages, and the 'Q_not' node voltage). Adding enough transistors to reset each of these voltages to 0 will certainly get the job done but may be overkill; each transistor you add will be another transistor that you will have to eventually include in your layout so it is advantageous to add as few transistors as possible.

Misc

- You do not have to do any layout for this assignment (this will be assigned in a later lab).
- You must create a Cadence schematic for you FF that has the asynchronous reset added.