

Why Does Power Matter?

Agenda

- Introduction
- Power in low-end applications
- Power in high-end applications
- Designing for power
- Conclusion

Applications Demand Lower Power

Low-End Applications

Example:

- Portable media players
- Modems and customer's premises equipment (CPE)
- Software-defined radio

- **Battery operated**
- **Form factor restrictions**
- **Operating conditions**

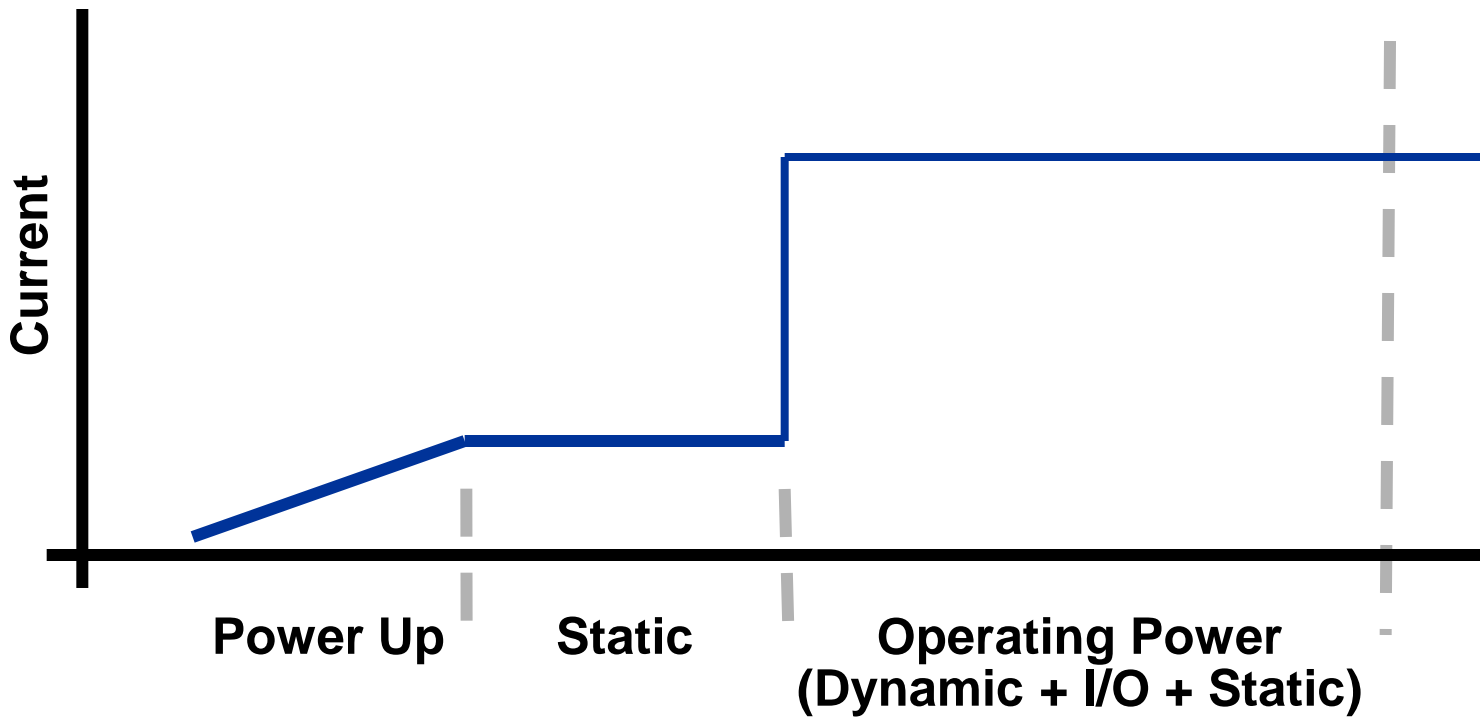
High-End Applications

Example:

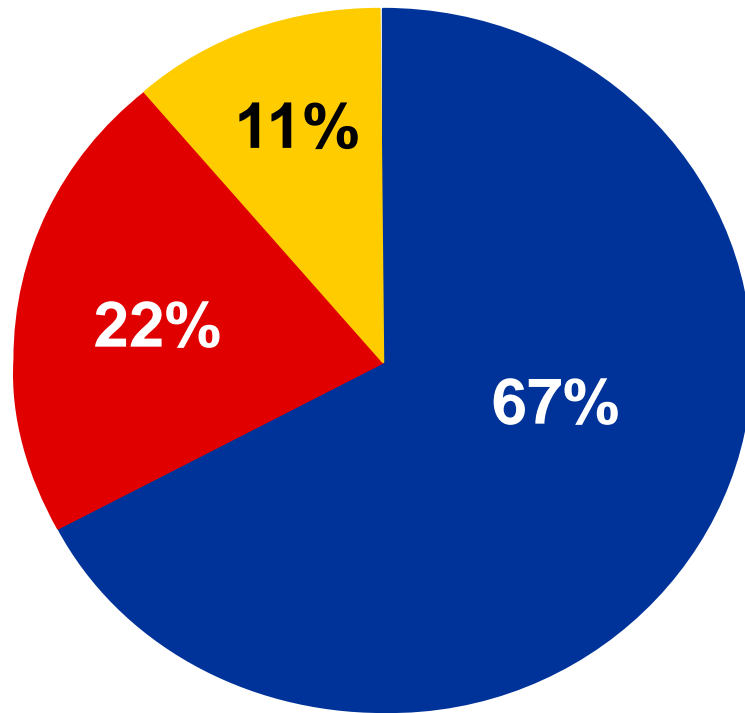
- Core routers
- Backplanes
- High-performance digital signal processing (DSP)

- **High performance**
- **New process nodes**
- **Operating conditions**

Power in PLDs



Operating Power



Analysis of 99 User Designs

- Core dynamic
- Core static
- I/O

Dynamic Power Dominates

```
nbit_adder: adder1
    GENERIC MAP (K => 8)
    PORT MAP (AddSubR_n => AddSubR_n, M => M);
multiplexer: mux2to1
    GENERIC MAP (K => 8)
    PORT MAP (A_in => Z_ADDER_OUT, B_in =>
AddSubR_n <= (OTHERS => AddSubR_n)
M <= (OTHERS => XOR_ADDER_OUT) XOR M(n-1);
```

Power in Low-End Applications

Low-End Applications

- Meet customer performance and power/thermal requirements simultaneously
- Eliminate or reduce cost of cooling systems
- Enable operation in thermally challenged and space-constrained environments
 - Airplane cockpits, software-defined radios
- Extend battery life for portable applications

Portable Applications

Point of Sale

- Scanners
- RF identification device (RFID)
- Tax collection
- Credit checks
- ATM PIN terminal



OS processor

- Industrial PDA
- Test equipment
- Remote terminal
- GPS
- Portable media player



Everything wireless

- Bluetooth
- Wireless fidelity (WiFi)
- 802.11x
- Headphones
- Camera
- Game controllers

Sensors

- Gas
- Temperature
- Machine-vision
- Location/GPS
- RF signal
- RFID

Portable Applications and Requirements

Applications	Requirements		
	3.3 V	High I/O Count	High Density
Consumer handheld (Educational toys and portable media players)	✓	✓	✓
Handheld instrumentation (Bar code scanners and handheld testers)	✓	✓	
Industrial computer (Meter readers and industrial PDAs)	✓	✓	✓
Industrial cameras (Camera modules)	✓	✓	
Wireless and wireline (Optical modules and PCMCIA express cards)	✓	✓	

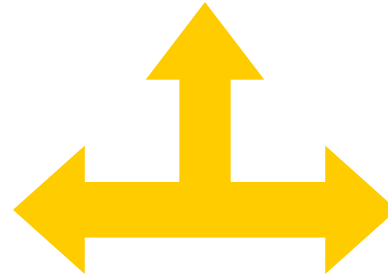
Portable Design Challenges

Cost

- System integration
- Power rails

Power

- Battery life



Size

- Board space

Low-Power Considerations

- Reduce power consumption in devices
 - How portable, consumer products designers model power consumption
 - Using this model to evaluate CPLDs
- Manage power for entire system
 - Self power down
 - Auto power up
 - Power management

Power Consumption Model

Mode	Definition	Power Consumption
Active	Part is being used	Dynamic power Application dependent
Standby	Part is powered, but not being used	Static I_{CC} , but only valid if no inputs are switching
Sleep/ Hibernate	Inactive, but retains information	< 50 - 100 μ A
Off	Powered off	Zero power

Static I_{CC} Is Difficult to Achieve

- Low static I_{CC} depends on:
 - Small density: limits PLD usefulness
 - Quiescent I/Os: but “don’t care” inputs are often toggling
- Customers prefer to power off the device when not used

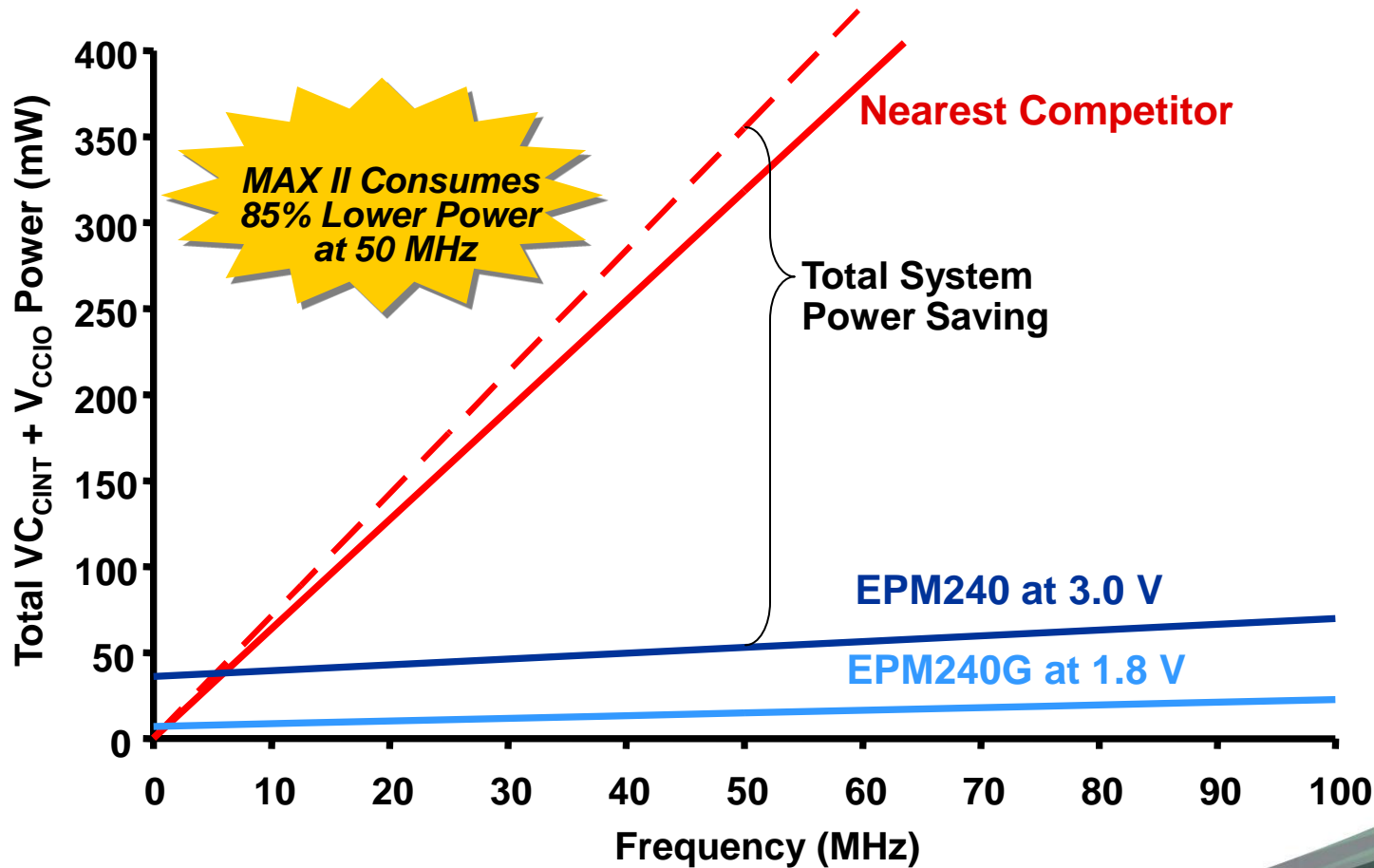
Off Mode Constraints

- CPLD core and I/O can be powered off and on in any sequence
 - Outputs must not affect the system operation
- When CPLD is powered off, inputs can be driven with
 - No damage to part
 - No power consumption

MAX[®] II CPLDs in Off Mode

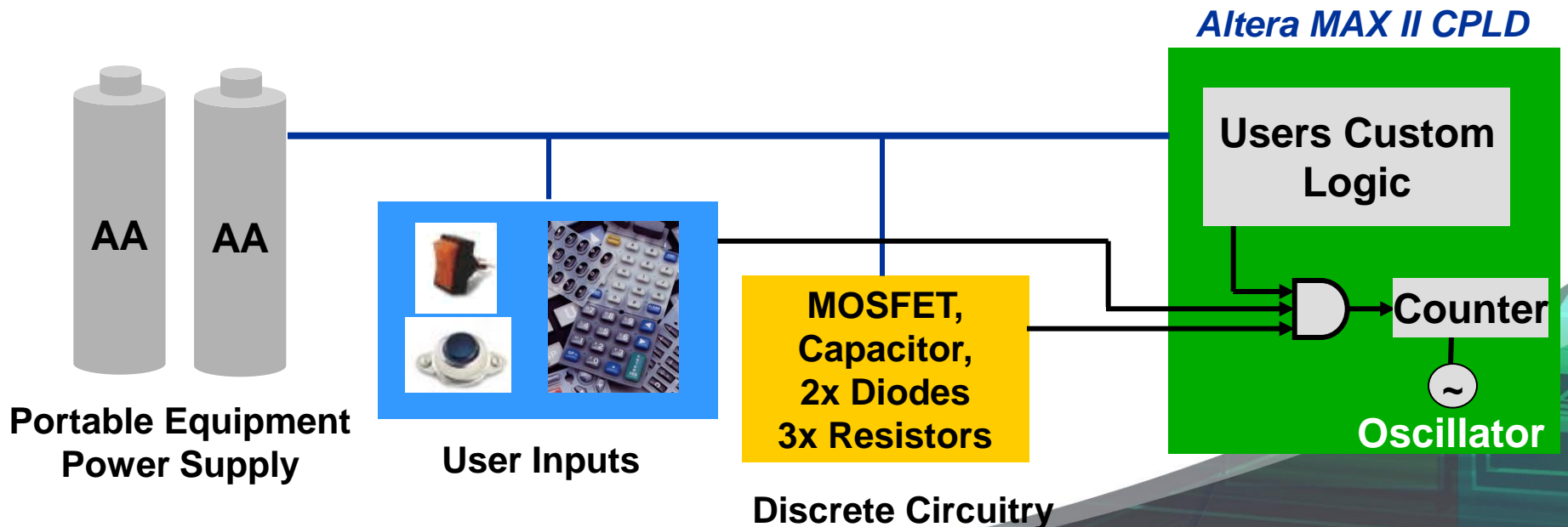
- No power sequence requirements
 - Outputs: stable and do not affect the rest of the system
- Well-behaved I/O
 - Active inputs: no damage
 - Active inputs: no power consumption

Dynamic Operation Power Consumption



CPLD Power-Down Mode

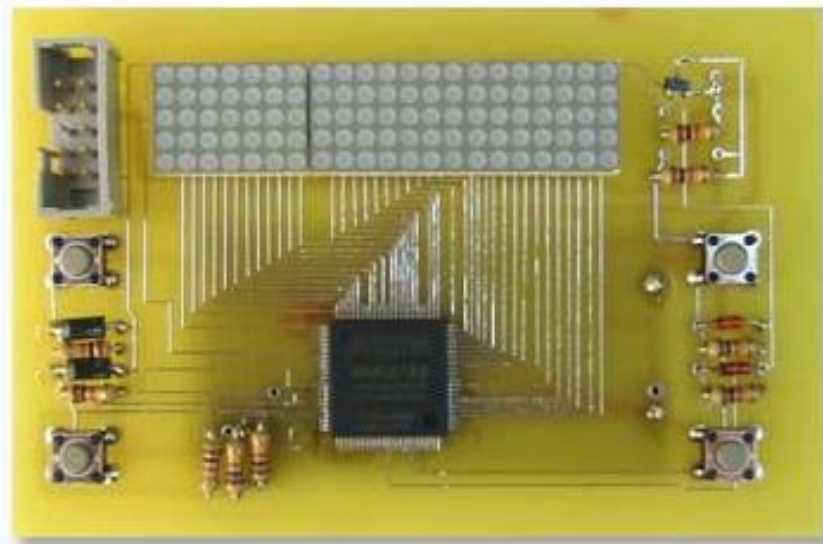
- Auto power down and instant-on (300 us)
- Internal oscillator makes system self contained
- Hot socket + power down mode
 - OK to drive CPLD I/Os: no damage and no power consumption
- Concept can be expanded to overall system power management



MAX II Power-Down Mode Design

- Application note and design files

Available
Now



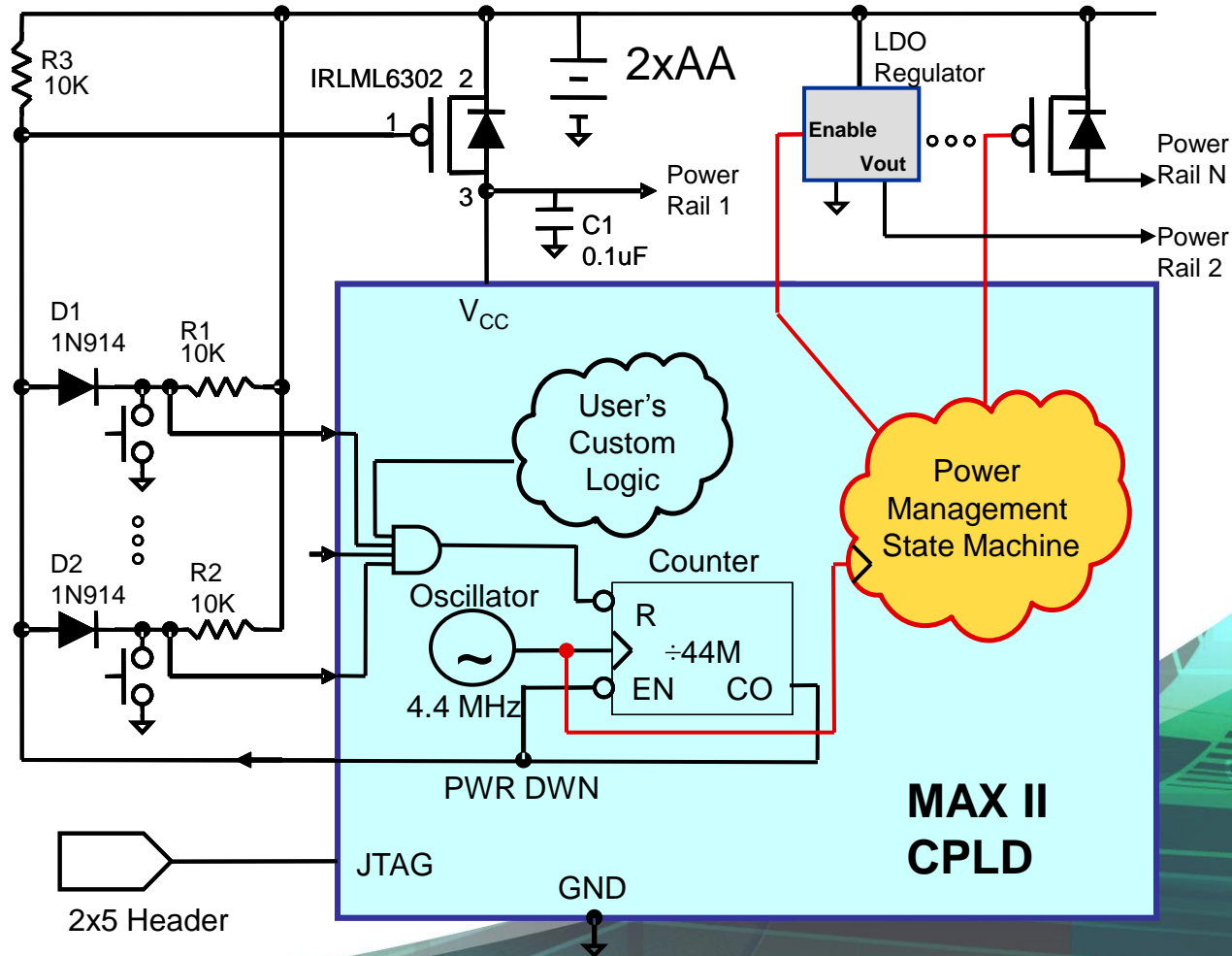
Front



Back

Controlling System Power

- Extend MAX II power-down design to include complete system power management
- MAX II CPLD is always the first to power up and the last to power down




```
nbit_adder: adder1
    GENERIC MAP (x => 8)
    PORT MAP (AddSubR_n => 0, M_n => 0)
multiplexer: mux2to1
    GENERIC MAP (x => 1)
    PORT MAP (A_in => Z, S_in => G
AddSubR_n <= (OTHERS => 0) AddSubR_n
M_n <= (OTHERS => 0) XOR AddSubR_n
M_n <= (OTHERS => 0) XOR G_n XOR M_n-1);
```

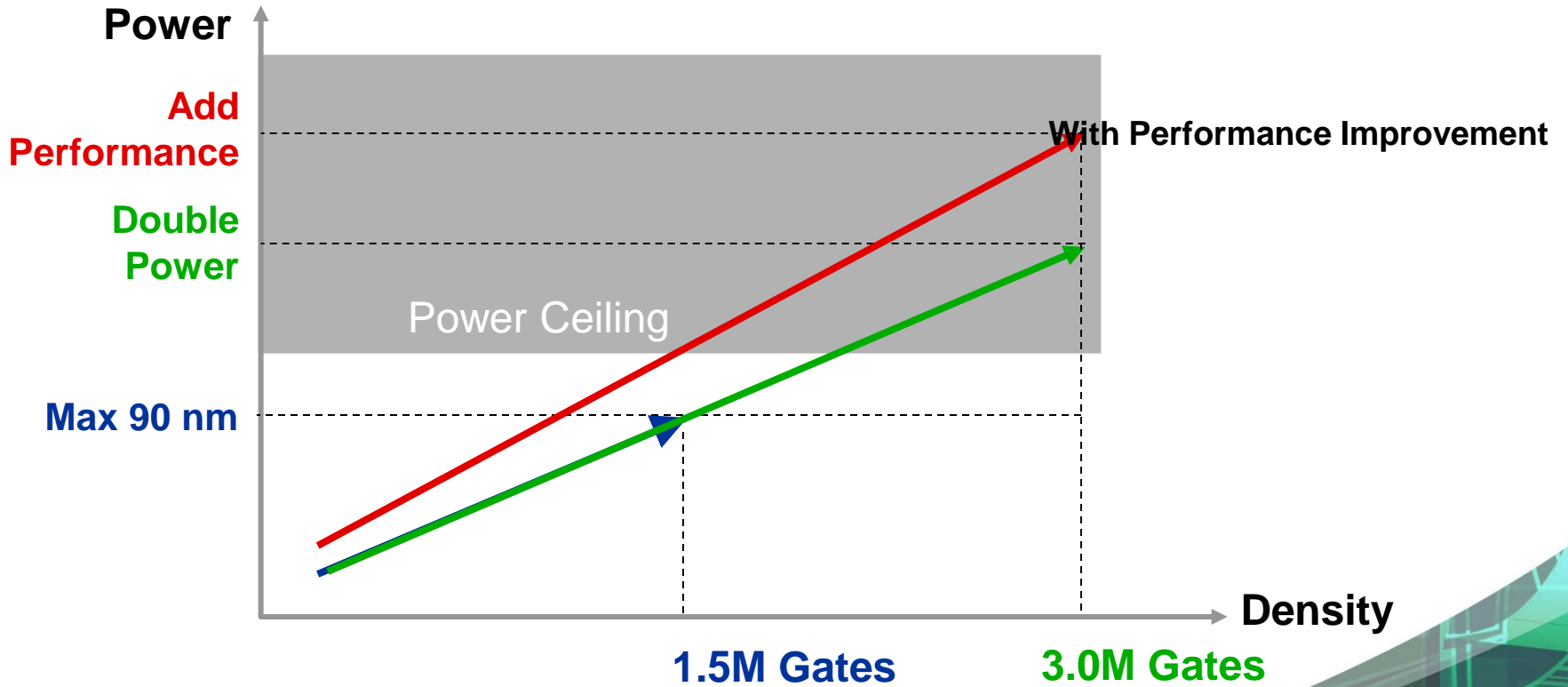
Power in High-End Applications



Factors Affecting Power

- New process technologies
 - Voltage and dimension scaling
 - Silicon characteristic changes
 - Novel materials used
- Higher performance and higher density
 - Affects dynamic power
 - Process changes
 - Geometry shrink

Power Challenge



Power limitations for applications while scaling

Leading Edge Process Technology

Process or Design Technology	When Altera Introduced	Benefit
All Copper Routing	180nm	Increased performance
Low-K Dielectric	130nm	Increased performance Reduced power
Multi-Threshold Transistors	90nm	Reduced power
Variable Gate-Length Transistors	90nm	Reduced power
Triple Gate Oxide	65nm	Reduced power
Super-thin Gate Oxide	65nm	Increased performance
Strained Silicon	65nm	Increased performance

Leading-Edge Process Technology

Increased Performance, Reduced Power

- Advanced 65-nm process
 - 15% capacitance reduction → reduces dynamic power 15%
- Strained silicon
 - Increased performance
- Multiple-gate oxide thicknesses (triple oxide)
 - Tradeoff: power vs. speed per transistor
- Multiple-threshold voltages
 - Tradeoff: power vs. speed per transistor
- Low-k inter-metal dielectric
 - Reduces dynamic power, increases performance
- Copper interconnect
 - Increased performance, reduced IR drop

Altera at 65 nm

- Maximum performance with minimum power
 - Innovative architecture and circuit techniques
 - The latest process optimizations
 - Integrated software solutions
- Customers get:
 - Performance they need with the minimum power
 - High productivity with automated tools that meet target performance and minimize power

Industry-Leading Low-Power Technology

Stratix® III Power Reduction Technique	Lower Static Power	Lower Dynamic Power
Silicon Process Optimizations	✓	✓
Programmable Power Technology	✓	✓
Selectable Core Voltage (0.9 V or 1.1 V)	✓	✓
Quartus® II PowerPlay Power Optimization		✓

Stratix III FPGAs Are the Lowest Power High-End FPGAs Available

Individual Block Optimization

- All core blocks completely redesigned for 65-nm process AND power reduction
 - Adaptive logic module (ALM), memories, DSP, CRAM, etc.
- Every mode of operation is optimized for:
 - AC: Least amount of switching activity
 - DC: Low-power mode setting for all unused circuitry
- Combined hardware hooks and Quartus II software intelligence to achieve power savings

Dynamic Power

- Process reduction reduces capacitance and voltage

$$P_{dynamic} = \left[\frac{1}{2} CV^2 + Q_{ShortCircuit} V \right] f \cdot activity$$

Capacitance charging

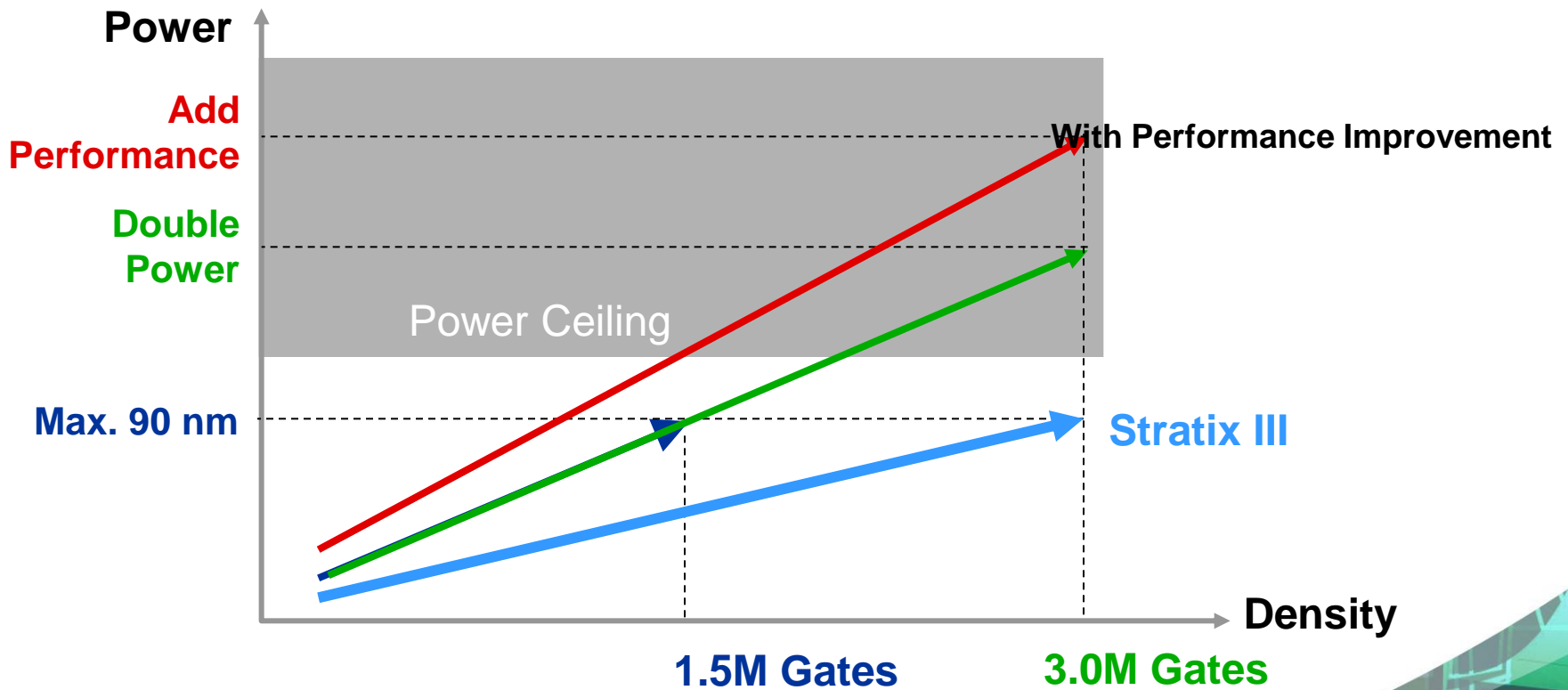
Short circuit charge during switching

Percentage of circuit that switches each cycle

15% Reduced Capacitance

- 15% power reduction proportional to reduction in capacitance
- Source of lower capacitance
 - Process scaling
 - Design improvements

Power Challenge



Stratix III FPGAs Cut Power by 50% vs. 90 nm

Selectable Core Voltage

- User selects core voltage operation
 - 0.9 V* or 1.1 V

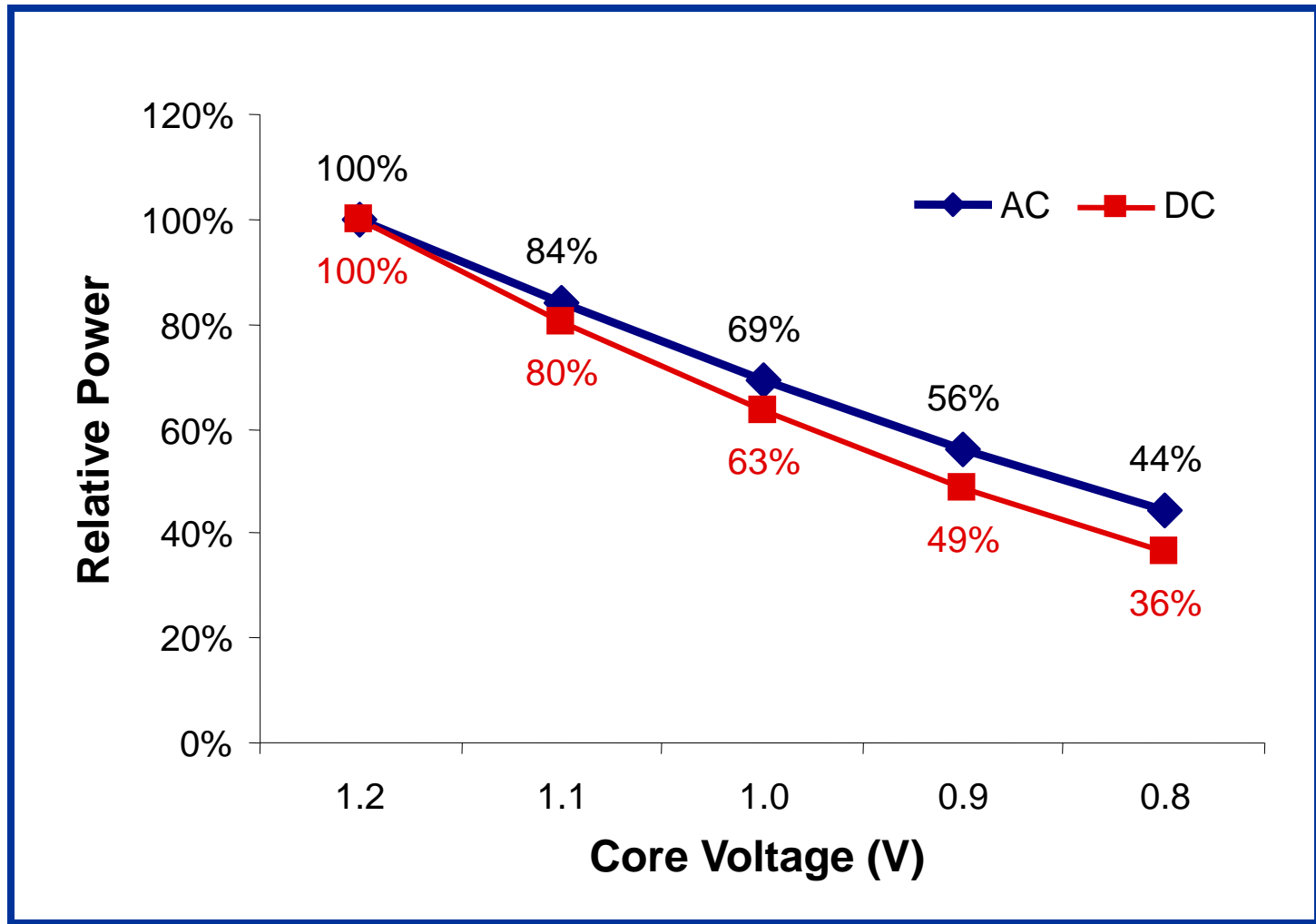
Core Voltage	Dynamic Power Reduction** from 1.2 V	Static Power Reduction*** from 1.2 V
1.1 V	16%	20%
0.9 V	44%	51%

* 0.9 V requires an additional power supply

** Dynamic power decreases by square of voltage reduction

*** Static power decreases by $\wedge 2.5$ of voltage reduction

Core Voltage Component

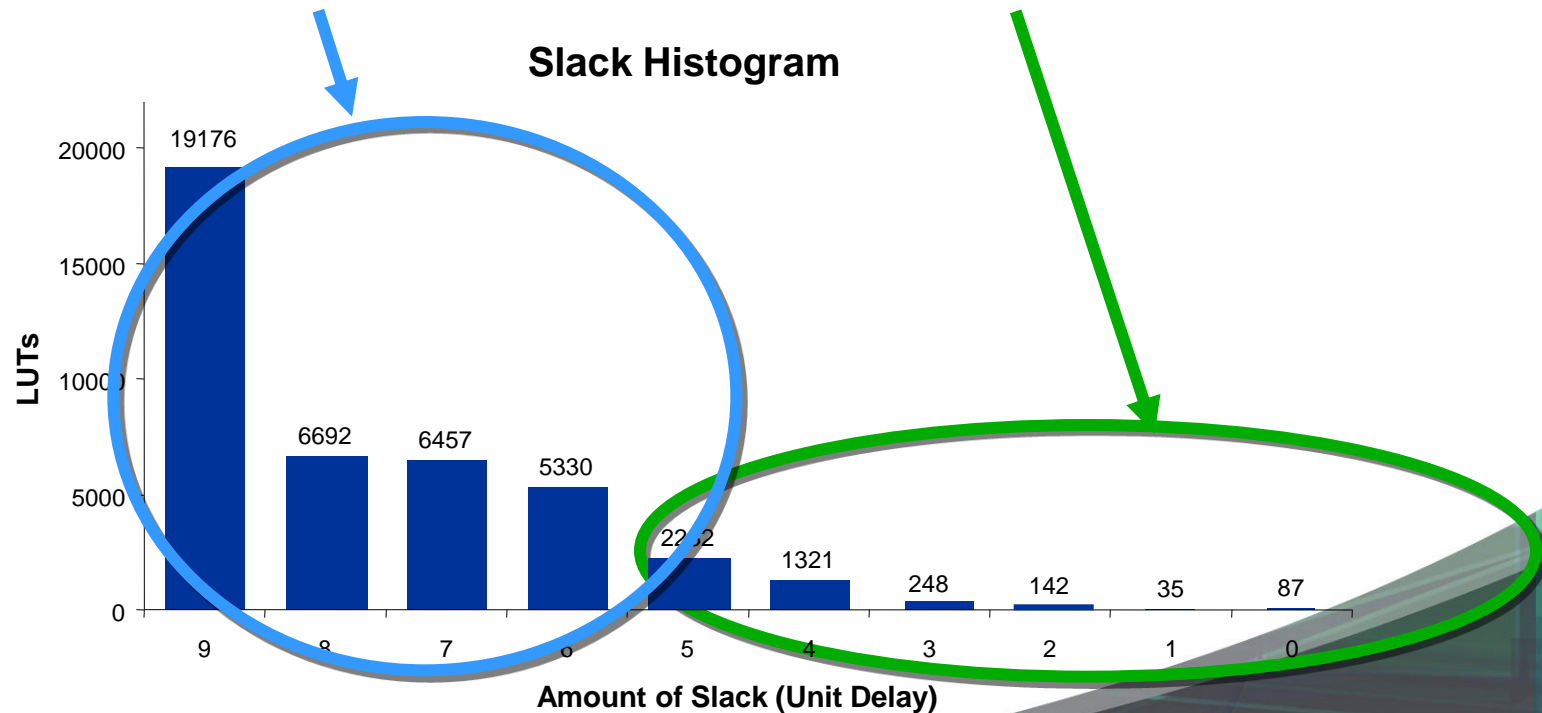


Design-Specific Power Optimization

- Only a small proportion of logic is performance-critical

Low Performance Requirements

High Performance Requirements

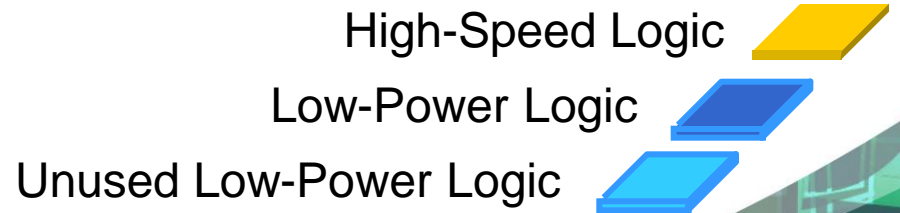
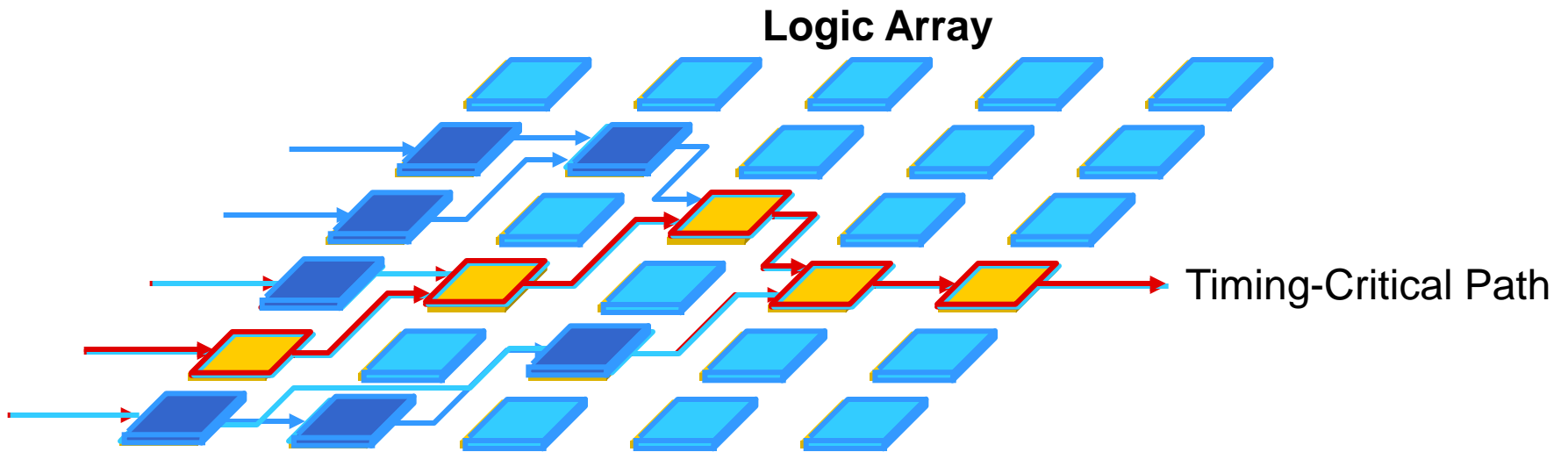


Programmable Power Technology

- Block-level adjustments lower total power consumption
 - Automatically programmed via Quartus II software based on design's performance requirements
- Puts the performance where you need it
 - Minimizes power everywhere else
- Patented techniques exclusively used by Altera

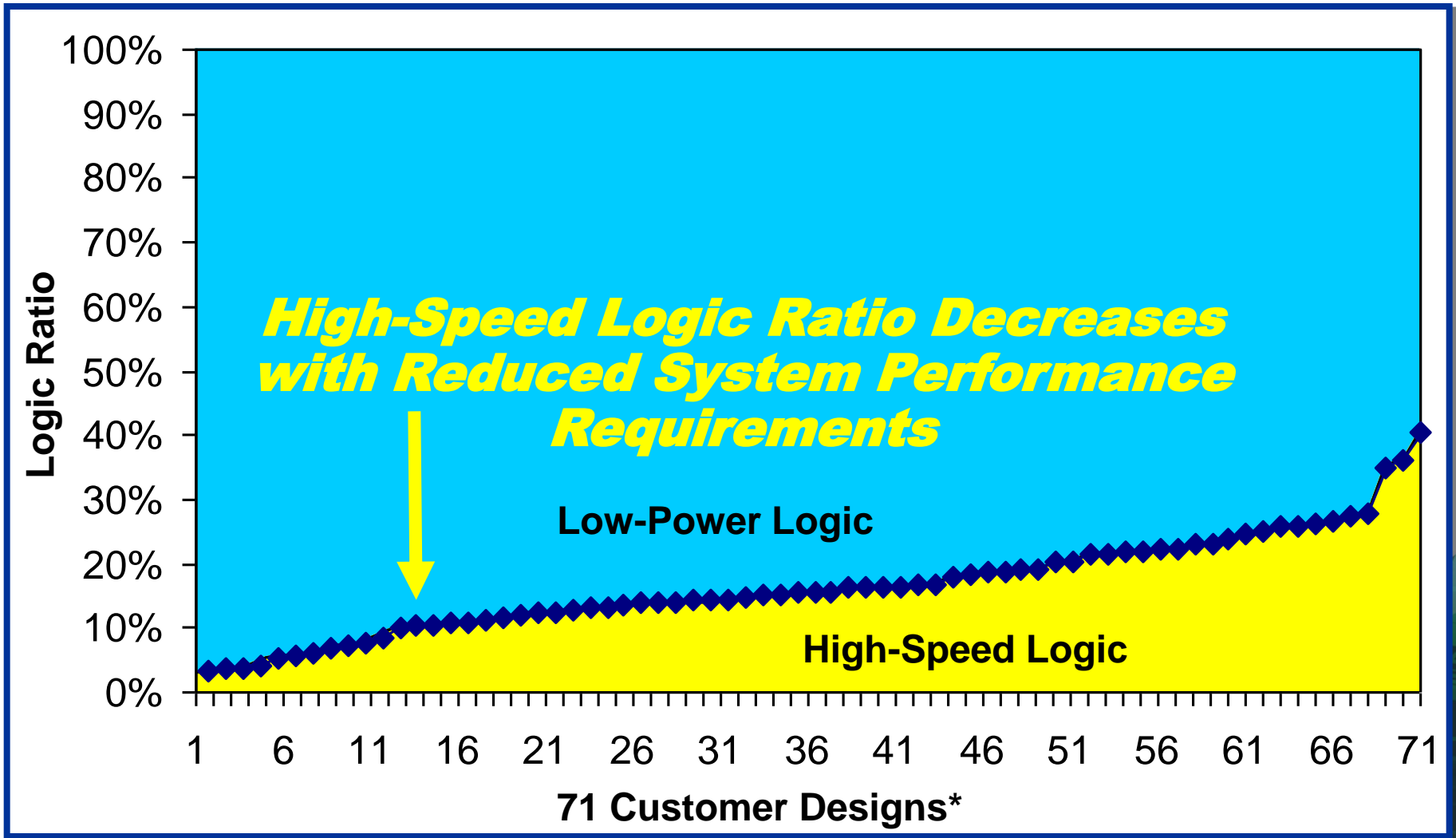
***Reduces Power Without
Impacting Performance***

Programmable Power Technology



***Performance Where You Need It,
Lowest Power Everywhere Else***

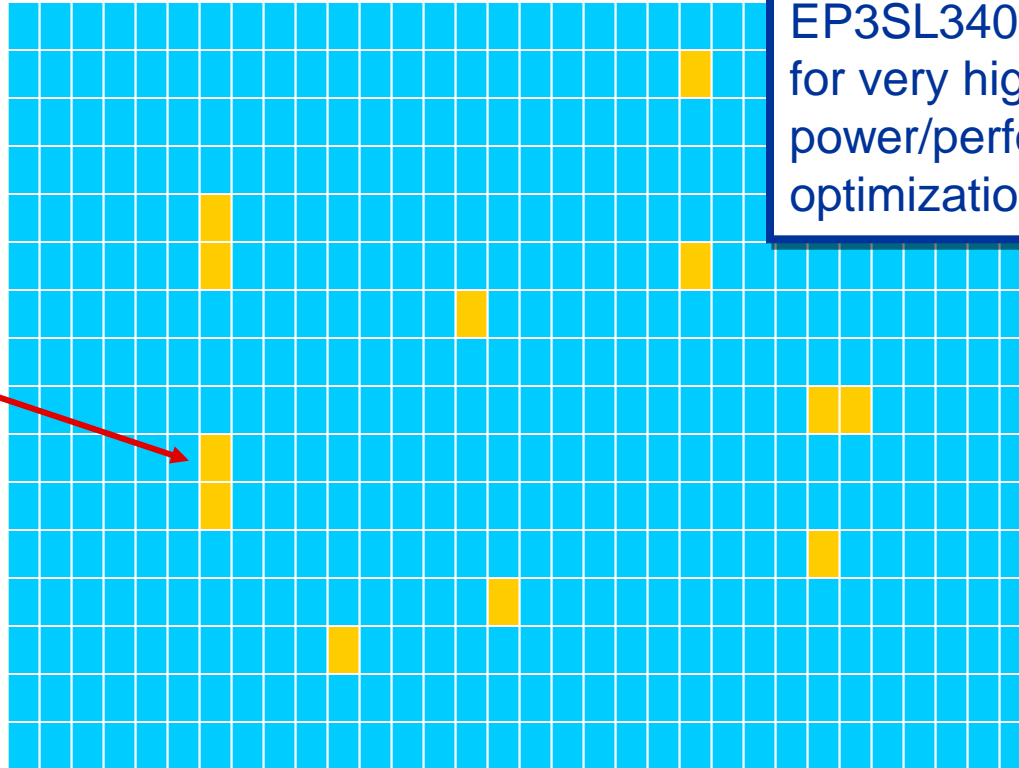
High-Speed vs. Low-Power Logic



*All designs compiled for maximum performance.

High-Resolution Power Control

EP3SL340 has 13,500 LABs for very high-resolution power/performance optimization



Only small % of LABs need to be fast to maintain the system performance

***Speed of the Fastest LABs,
Power of the Slowest***

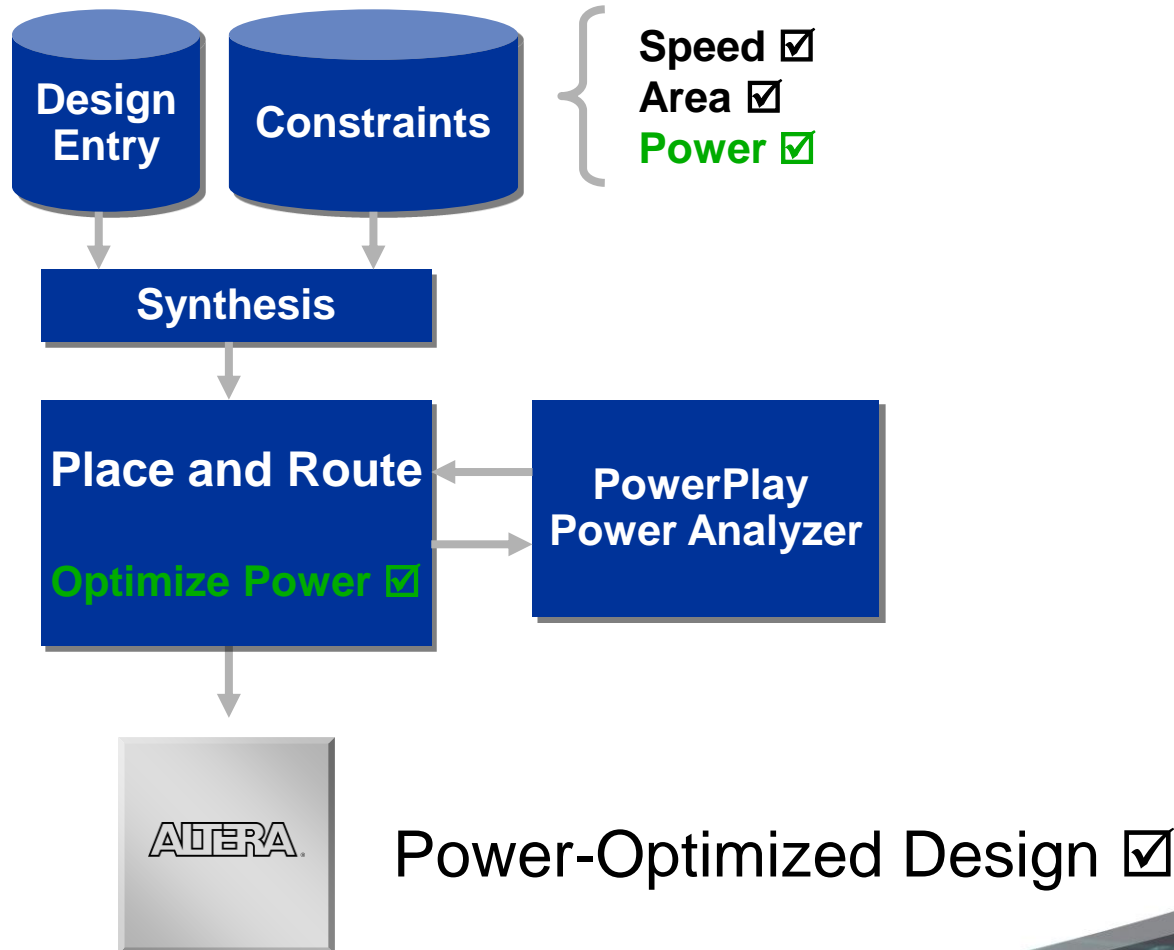
```
nbit_adder: adder1
    GENERIC MAP [ n => 8 ]
    PORT MAP [ AddSubR_n => A, B, C, D, E ]
multiplexer: mux2to1
    GENERIC MAP [ n => 8 ]
    PORT MAP [ A_in => A, B_in => B, C_in => C, D_in => D, E_in => E,
    AddSubR_n <= (OTHERS => AddSubR_n)
    MUX_n <= A XOR AddSubR_n
    MUX_n <= B XOR AddSubR_n
    MUX_n <= C XOR AddSubR_n
    MUX_n <= D XOR AddSubR_n
    MUX_n <= E XOR AddSubR_n
    MUX_n <= M(n-1);
```

Designing for Power

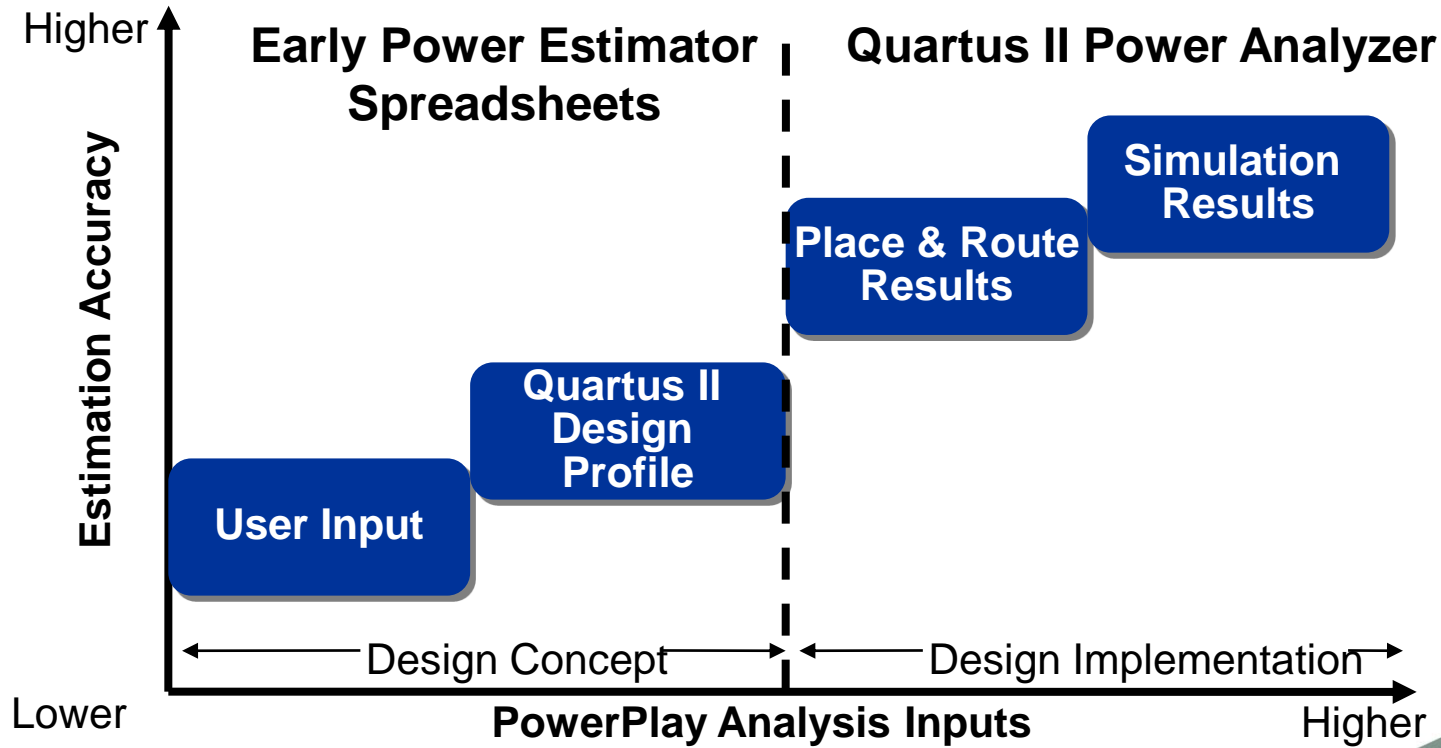
Designing For Power

- Need to plan for power right from the beginning of the design
 - Cannot wait until board bring-up
- Design tools available for managing power in FPGAs
 - PowerPlay Analyzer
- Power-based design optimization possible
 - PowerPlay Advisor

Automated Power Optimization

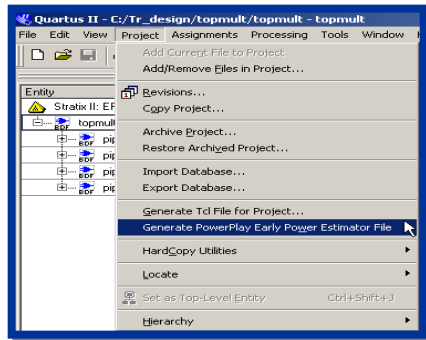


PowerPlay Power Analysis Tools



PowerPlay Early Power Estimator

- Quartus II software generates file and macro to import into web-based Excel spreadsheet
- Can estimate performance for partially complete designs
 - User can modify number of logic elements (LEs), etc. in Excel
 - Computes power as a function of number of LEs, I/Os, clock frequencies, activities, etc.



PowerPlay Early Power Estimator spreadsheet imports text file.



HSDI									
IO Domain	Data Rate (Mbps)	# of Channels	Issues (mA)	Issues (mW)	Power (mW)	Power (mW)	Power (mW)	Power (mW)	Power (mW)
0	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
1	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
2	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
3	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
4	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
5	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
6	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
7	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
8	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
9	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
10	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
11	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
12	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
13	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
14	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
15	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
16	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
17	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
18	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
19	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
20	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
21	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
22	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
23	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
24	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
25	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
26	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
27	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
28	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
29	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
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31	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
32	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
33	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
34	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
35	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
36	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
37	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
38	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
39	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
40	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
41	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
42	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
43	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
44	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
45	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
46	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
47	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
48	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
49	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
50	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
51	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
52	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
53	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
54	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
55	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
56	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
57	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
58	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
59	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
60	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
61	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
62	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
63	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
64	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
65	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
66	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
67	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
68	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
69	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
70	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
71	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
72	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
73	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
74	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
75	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
76	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
77	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
78	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
79	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
80	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
81	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
82	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
83	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
84	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
85	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
86	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
87	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
88	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
89	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
90	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
91	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
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95	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
96	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
97	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
98	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
99	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
100	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
101	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
102	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
103	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
104	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
105	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
106	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
107	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
108	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
109	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
110	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
111	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
112	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
113	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
114	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
115	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
116	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
117	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
118	0	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
119	0	0	0.00	0					

PowerPlay Power Analyzer

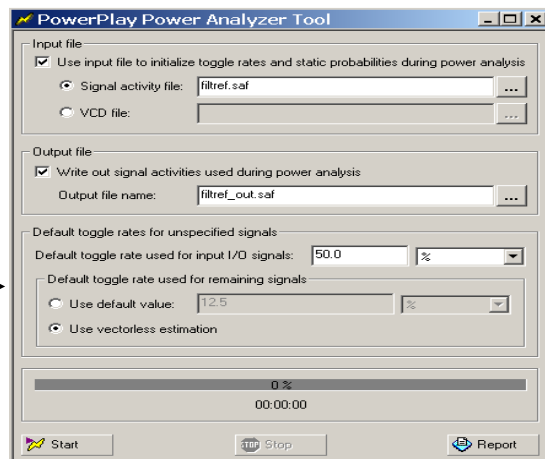
User Inputs

RTL or Timing Simulation (VCD*)

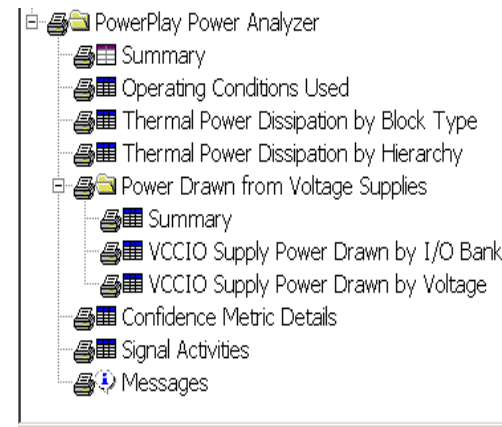
Default Node Activity

Operating Conditions

PowerPlay Analyzer



Reports

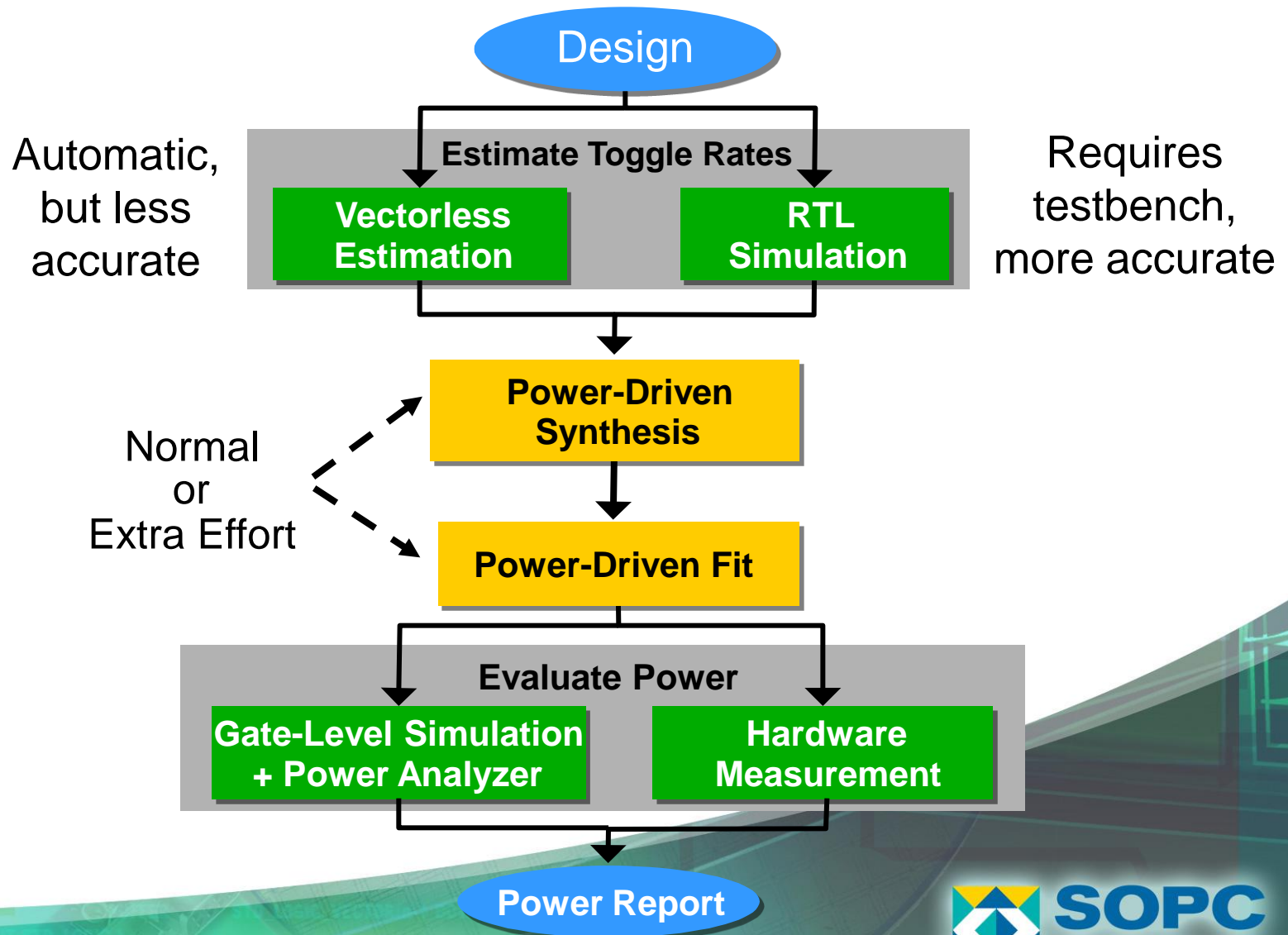


- Power models
- Place-and-route results
- Vectorless activity rates

Analyze Power

*VCD: Vector Change Description

PowerPlay Power Optimization



Power Optimization Advisor

- Recommended settings and design changes to minimize power



The screenshot shows the 'Power Optimization Advisor' dialog box. The left pane shows a tree view with 'Clock Enables on Logic' selected. The right pane displays the following information:

Clock Enables on Logic	
Recommendation	Whenever logic is not used on a significant fraction of clock cycles, specify a clock enable in your design HDL, schematic or megafunction instantiations so that the appropriate registers are shut down on these cycles.
Description	Using a clock enable to shut down registers reduces power even when the data input to those registers is not changing on a given clock cycle, since the portion of a clock inside the LAB or DSP block is shut down by the enable, and hence clock power is reduced by clock enables. More Info
Summary	The following areas will be affected by the recommended changes: = Delay is unaffected (fmax is unaffected) = Logic element usage is unaffected = Compilation time is unaffected
Action	Write your Hardware Description Language (or other design entry format) code such that clock enables are used whenever appropriate on registers.

Conclusion

- Power optimization and power management is becoming a critical aspect of system design
- Stratix III FPGAs provide innovative programmable power technology for power optimization
- Industry leading PowerPlay tools from Altera enable optimum power

Thank You
Q & A