





Stratix HardCopy Design Flow With Quartus-II Ver. 3.0



Agenda

- HardCopy Stratix Overview
- Quartus II 3.0 Features For HardCopy
 - Compilation And Supported Devices
 - Design Assistant
 - HardCopy Optimization Wizard
 - HardCopy Timing Constraints
 - HardCopy Files Wizard
 - HardCopy Power Estimation
- Designing For HardCopy
 - Clock
 - Reset
 - Timing Closure
 - Non-synchronous Design Structure





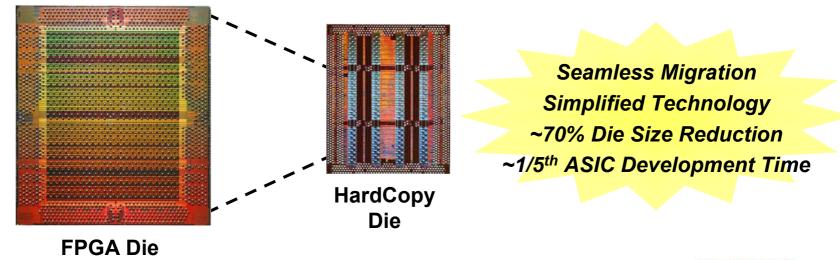


HardCopy Stratix Overview



Stratix HardCopy Value Proposition

- Industry's Only Complete Solution from Prototype to Production
 - Benefits of Designing with FPGAs
 - Seamless Migration from Proven FPGA Design to Custom Design
 - Unified & Complete Design Methodology with Single Design Tool
- Single Source for Devices, Tools & Intellectual Property (IP)

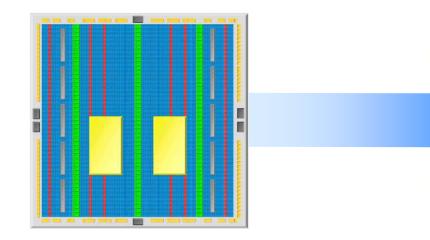




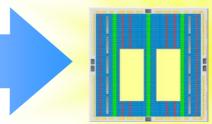


FPGA to HardCopy Device

- Remove Configuration Circuitry
- Remove Programmable Routing
- Remove Programmability for Logic & Memory
- Add Embedded Testability
- Customize with Two Metal Layers



FPGA Architecture with ASIC Routing



Stratix™ EP1S25

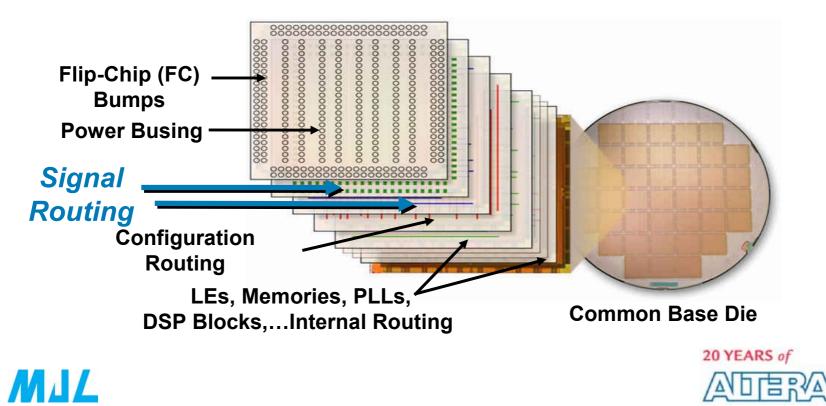
HardCopy HC1S25





HardCopy Silicon Technology

- Same Process Technology as FPGA
- Common Base Die
- Eight Metal Layers in HardCopy Stratix Devices
 - Two for Customer Design



INNOVATION

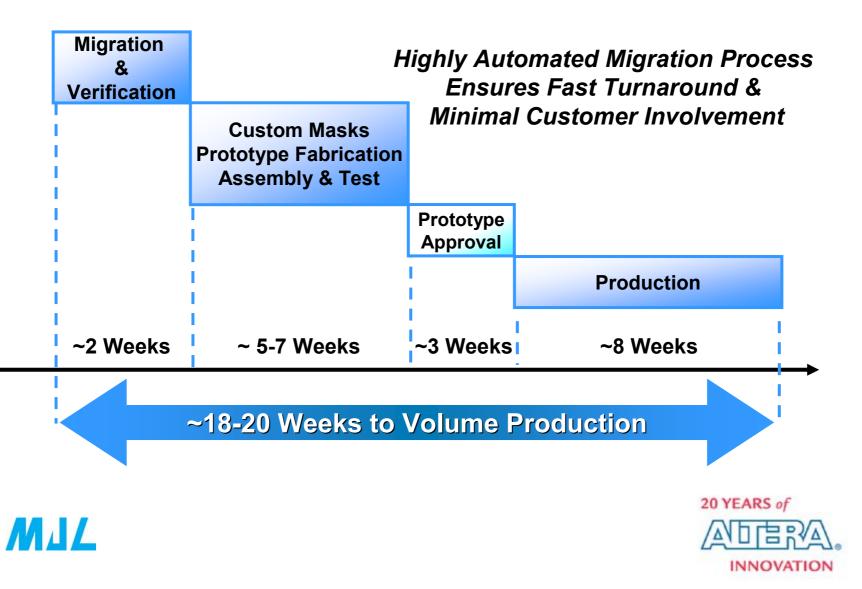
Verification

- Timing Verification
 - Industry-Standard Tools
 - Synopsys PrimeTime Tool
- Structural Verification
 - Boundary Scan, BIST
 - Automatic Test Pattern Generation (ATPG)
 - No Need for Functional Vectors from Customer
 - Ensures High-Fault Coverage, ~99%
- Altera Delivers Tested Devices

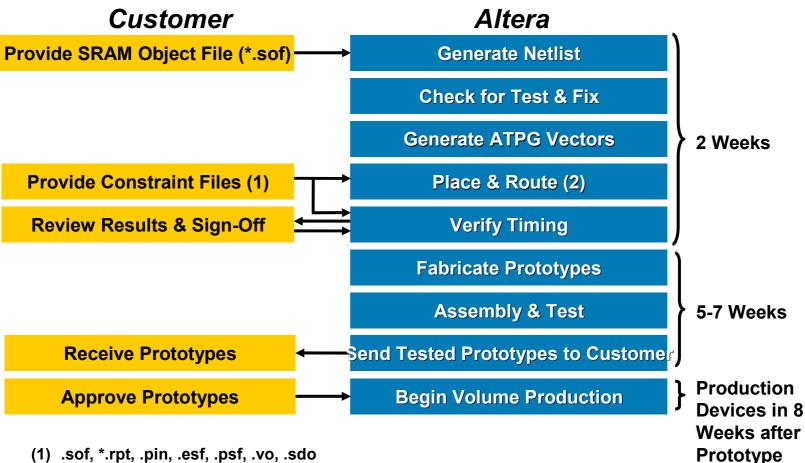




Implementation Timeline



Migration Flow



(1) .sof, *.rpt, .pin, .esf, .psf, .vo, .sdo

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- *.apc – Placement Constraint Files Optional

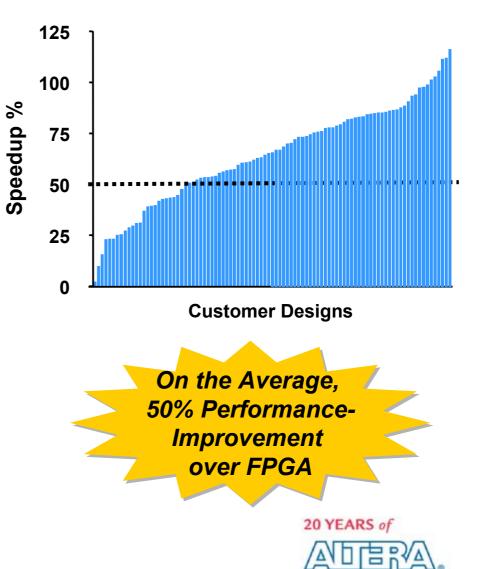
(2) Altera Will Use *.apc if Provided & Only Route Design



Approval

HardCopy Device Performance

- Smaller Die
- Routing Benefits
- Reduced Internal Delays
- I/O Speed Unchanged
- f_{MAX} Change Is Design-Dependent
- Performance Estimation through Quartus[®] II Software



INNOVATION



Power Benefits

~40% Lower Power Consumption than FPGA

- I/O Power Remains Unchanged
- Power Estimation Tool Supported by Quartus II Design Software
 - Also Available on Altera Web Site





HardCopy Vs. ASIC Devices

Category	HardCopy	ASIC
Design Time	2-3 Weeks	Months
Design Effort	Minimal	Significant
Investment in Tools	None	Significant
Staff Needed	None	Significant
Package Design Effort	None	Yes
Board Re-Design	No	Yes
Fabrication & Assembly Cycle Time	7 Weeks	12 Weeks
Non-Recurring Engineering (NRE) Cost	Low	High
Price per Part	Low	Lowest
Time to Volume	Weeks	Months

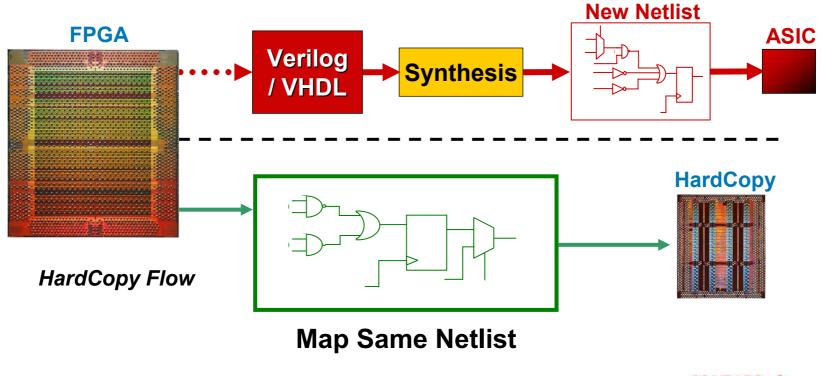
HardCopy Process Leverages the Benefits of FPGA Design & Engineering







ASIC Conversion Generates New Netlist Design Needs Validation & Adjustment



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ASIC Conversion Flow



HardCopy Migration Is Not ASIC Conversion

Altera FPGA	HardCopy	ASIC
Logic Elements	Same as FPGA	Re-Synthesis to Gates
Memory Blocks	Same as FPGA	Compiled/ Cell Based
I/O Pins	Same as FPGA	Different I/O Library
Phase-Locked Loops (PLLs)	Same as FPGA	Different Design
Intellectual Property	Same as FPGA	Re-Qualification & License
Packaging	Same as FPGA	Custom
Process Geometry	Same as FPGA	Same/Different/Hybrid
Foundry	Same as FPGA	Same/Different
Interconnect Routing	Similar SOG* of Sta	andard Cell ASIC Routing

* SOG – Sea of Gates

ASIC Conversion Requires Starting Over



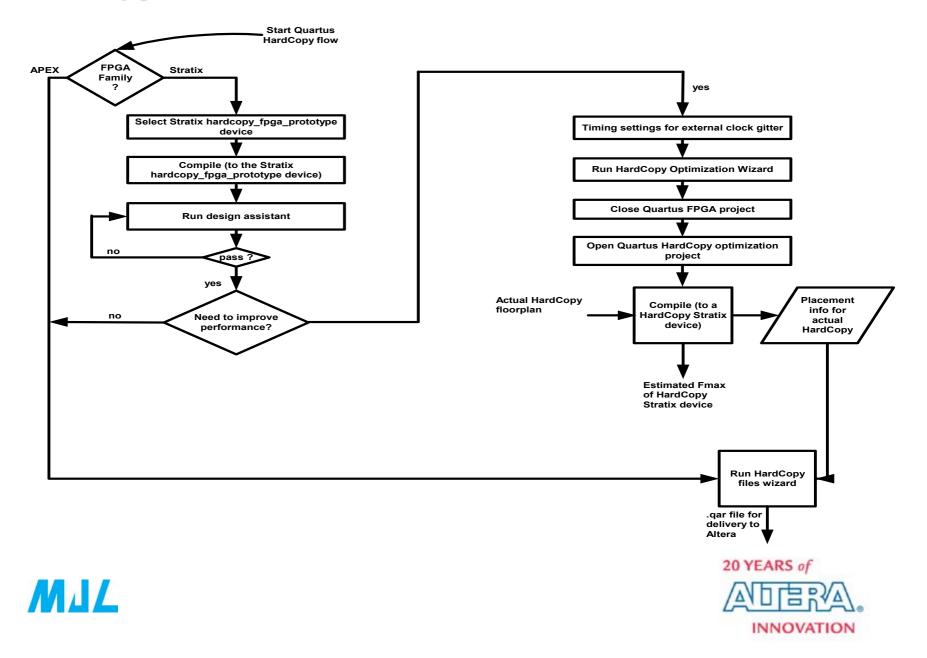




Quartus II 3.0 Features For HardCopy



HardCopy Process Flow



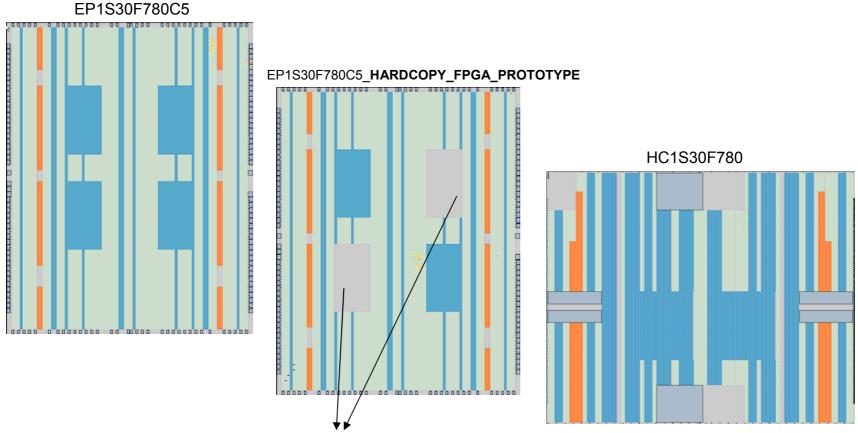
HARDCOPY_FPGA_PROTOTYPE Devices

- Part Of The Stratix Family
- Is A Virtual <u>FPGA</u> Device To Guide Quartus II
 - Has Reduced Feature Set From Its Equivalent FPGA
 - Less MRAMs As An Example
 - Has An Identical Timing Model As The FPGA
 - Has The Identical Floorplan Of The FPGA
- Is Not The Actual Hardcopy Device
 - Does Not Match The Floorplan Of The Hardcopy Device
 - Matches The Pin-out Of The Equivalent Hardcopy Device
- Always Has Equivalent Real FPGA
 - This Is NOT A New Hardware Die





HARDCOPY_FPGA_PROTOTYPE vs. FPGA vs. HardCopy devices



Blanked out MRAM blocks





Device Mapping

Physical FPGA	FPGA Prototype Device for HardCopy	HardCopy Device
EP1S25F672C6	EP1S25F672C6_HARDCOPY_FPGA_PROTOTYPE	HC1S25F672
EP1S25F672C7	EP1S25F672C7_HARDCOPY_FPGA_PROTOTYPE	ПС1525F0/2
EP1S30F780C5	EP1S30F780C5_HARDCOPY_FPGA_PROTOTYPE	
EP1S30F780C6	EP1S30F780C6_HARDCOPY_FPGA_PROTOTYPE	HC1S30F780
EP1S30F780C7	EP1S30F780C7_HARDCOPY_FPGA_PROTOTYPE	
EP1S40F780C5	EP1S40F780C5_HARDCOPY_FPGA_PROTOTYPE	
EP1S40F780C6	EP1S40F780C6_HARDCOPY_FPGA_PROTOTYPE	HC1S40F780
EP1S40F780C7	EP1S40F780C7_HARDCOPY_FPGA_PROTOTYPE	
EP1S60F1020C6	EP1S60F1020C6_HARDCOPY_FPGA_PROTOTYPE	HC1S60F102
EP1S60F1020C7	EP1S60F1020C7_HARDCOPY_FPGA_PROTOTYPE	0
EP1S80F1020C6	EP1S80F1020C6_HARDCOPY_FPGA_PROTOTYPE	HC1S80F102
EP1S80F1020C7	EP1S80F1020C7_HARDCOPY_FPGA_PROTOTYPE	0





Stratix Supported Devices

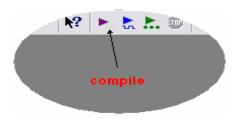
Table 1: Hardcopy Stratix Devices Vs. Equivalent Stratix Devices							
	Resources Compared to Equivalent FPGA						
Device	LEs	M512 Blocks	M4K Blocks	M- RAM Blocks	DSP Blocks	PLLS	Max. User I/Os
HC1S25F672	25,660	224	138	2	10	6	473
EP1S25F672	25,660	224	138	2	10	6	473
HC1S30F780	32,470	295	171	2	12	10	597
EP1S30F780	32,470	295	171	4	12	10	597
HC1S40F780	41,250	384	183	2	14	12	615
EP1S40F780	41,250	384	183	4	14	12	615
HC1S60F1020	57,120	574	292	6	18	12	773
EP1S60F1020	57,120	574	292	6	18	12	773
HC1S80F1020	79,040	767	364	6	22	12	773
EP1S80F1020	79,040	767	364	9	22	12	773

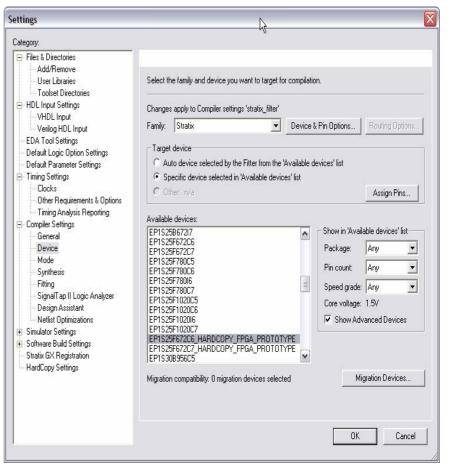




Compilation

- In An Open Project, Select The Target HardCopy Device Thru The Compiler Setting Option. Make Sure To Select a HARDCOPY_FPGA_PROTOTYPE device
- Assignments -> Device Menu Option Will Bring You To The Settings Window
- Compile Your Design









Design Assistant

Design Assistant Checks Your Design Against Design Rules That Are Selected Thru The Assignment Menu. Turn It On During Compilation.

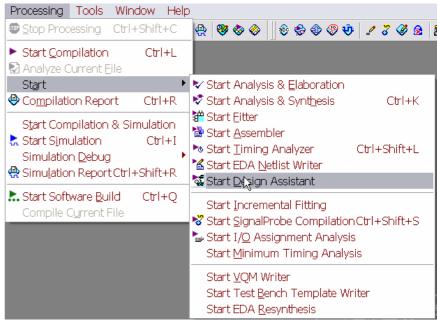
Assignments	Settings	
 Device Assign Pins Ijiming Settings EDA Tool Settings Settings Settings Ctrl+Shift+E Timing Wizard Gompiler Settings Wizard Software Build Settings Wizard Software Build Settings Wizard Assignment Editor Ctrl+Shift+A Remove Assignments Demote Assignments Back-Annotate Assignments Back-Annotate Assignments Last Compilation Floorplan Timing Closure Eloorplan 	Category: Category: Add/Remove User Libraries Toolset Directories HDL Input Settings VHDL Input Default Logic Option Settings Default Logic Option Settings Default Parameter Settings Category Constant Default Parameter Settings Constant Cocks Other Requirements & Options Timing Analysis Reporting Compiler Settings General Device Mode Synthesis Fitting SignalTap II Logic Analyzer Design Assistant Netlist Optimizations Simulator Settings Stratix GX Registration HardCopy Settings	Specify options for the Design Assistant, which checks a design for potential design problems. Note: The availability of these options depends on the current device family. Changes apply to Compiler settings 'filtref' Run Design Assistant during compilation Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant configuration rule names Select the rules you want the Design Assistant to apply to the project. Select the rules you want the Design Assistant to apply to chara standard scheme Select the rule of the project the rule of the project to apply to the project t
Chip Editor Chip		OK Cancel

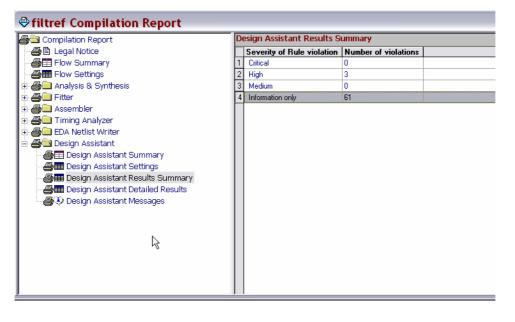




Design Assistant (Continue)

- Rules Are In Place To Guarantee Smooth Migration From FPGA To HardCopy Device
- Checks The Viability Of The Design And Assesses Its Risk
- Need To Make Sure All Violations Are Reviewed Informational Messages Are Acceptable









HardCopy Optimization Wizard

- HardCopy Will Always Perform As Good As FPGA. You May Not Need To Run Optimization Wizard Unless You Don't Meet Your Performance In FPGA
- The Optimization Wizard Is Used To Generate HardCopy Files That Will Approximate The Real Delays In The HardCopy Device
- The optimization wizard creates a new project directory, a .VSM file, and back-annotates the pin information from the original project.





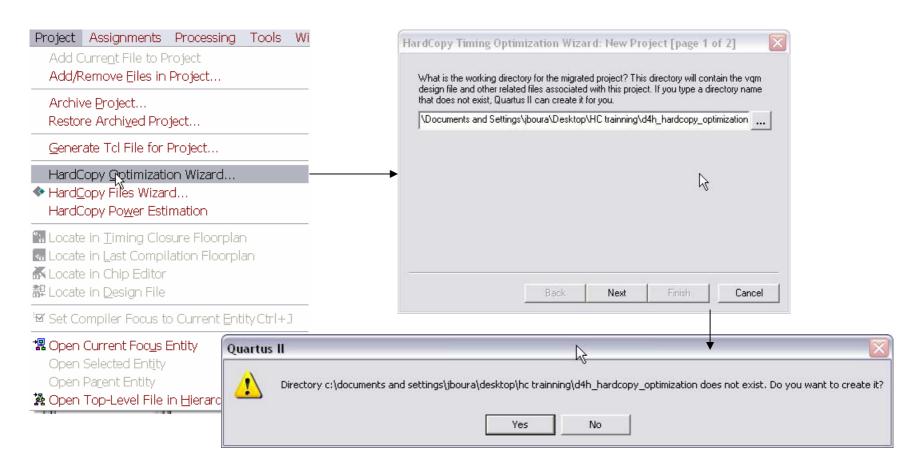
HardCopy Optimization Wizard (continue)

- All Pin Assignments Are Preserved.
- All Pin Properties Are Preserved
 - I/O Standard, Drive Strength, ...
- Global Assignments Are Maintained
- All Core Location Assignments Are Removed.
- All Logic Lock Regions Are Removed.
- All Timing Assignments Are Migrated
 - Including Multi-cycle, Point To Point Cuts, ...





HardCopy Optimization Wizard (Menu)







New Project

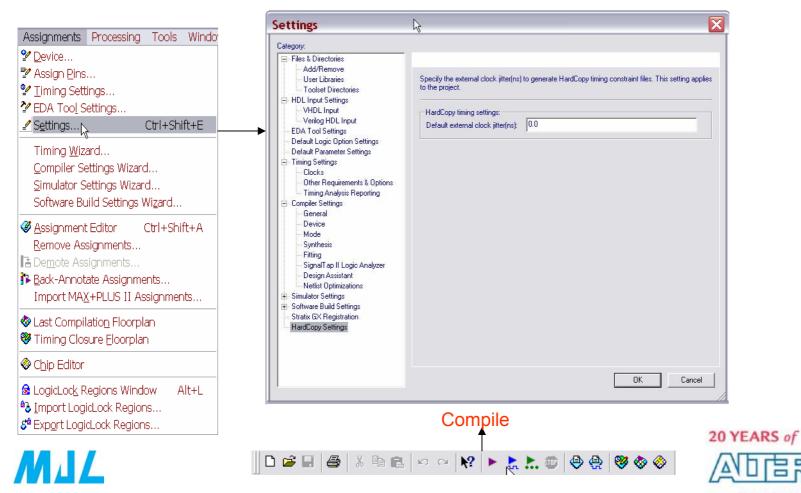
- We now have a new Quartus II Project in a new directory
 - Example: <my design>_hardcopy_optimization
 - Assigned to the equivalent Hardcopy member in the "Stratix Hardcopy" family.
- Old Quartus II project for FPGA_PROTOTYPE compile maintained
- Compiling the new project gives you the hardcopy timing estimation.
- Can change timing assignments
 - To optimize Hardcopy designs differently
 - To monitor timing differently





HardCopy Timing Constraints

In The New HardCopy Project Directory, Open The Project, Specify HardCopy Timing Constraint, Compile The Design, And Look Up The Timing Analyzer Results For The New FMAX.



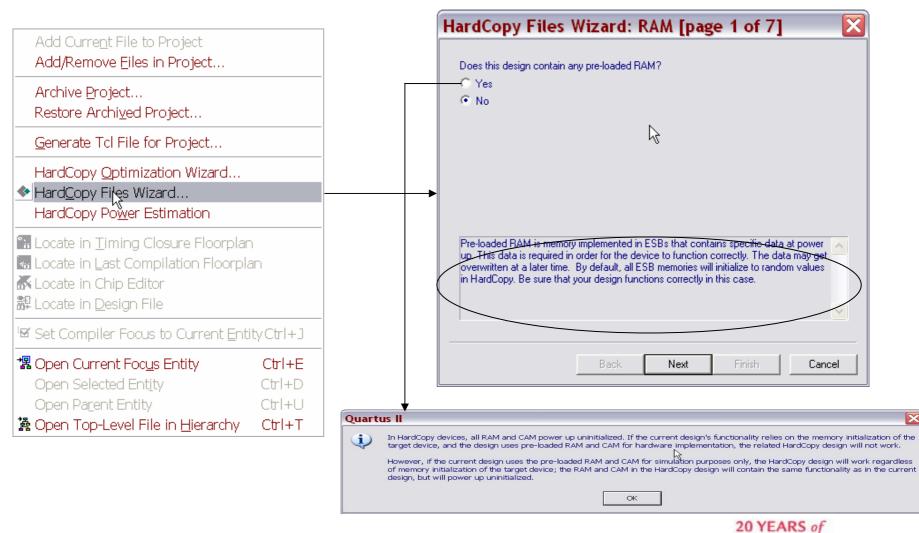
INNOVATION

HardCopy Files Wizard (formerly passport)

- The Files Wizard Could Be Run With Or Without An Optimization Run
- Runs Design Assistant With All Rules Enabled Regardless Of What The User Turned On/Off
- The Files Wizard Goes Thru An Interactive List Of Questions To Gather Design Specifications
- The Files Wizard Generates A .Qar File That Gets Sent To Altera For Conversion











HardCopy Files Wizard: SignalTap II [pa	age 2 of 🔀
Does this design use the SignalTap II Logic Analyzer?	Does this design's target device use JTAG BST?
C Yes	C Yes
© No	⊙ No
k − k	Does this design's target device use the JTAG user code
	C Yes
	C No
	Can Altera change the JTAG user code register?
	C Yes
	C No
function the same way that it does in the PLD. Back Next Finish	www.altera.com.If your design does not use the JTAG USERCODE register, then Altera will implement a specific number into that register for electronic identification of the HardCopy device. However, if you are using the JTAG USERCODE register, then Cancel Back Next Finish Cancel
	↓ Oursetur II
s II 🔀	Quartus II
	The JTAG BST order in HardCopy device is different than the order in the design's target device. Download the BSDL file for the H device from the Altera web site at
SignalTap II Lol Analyzer is disabled in HardCopy designs	device from the Altera web site at http://www.altera.com

Signal Tap Is Fully Supported In HardCopy Stratix, But Not In HardCopy APEX



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HardCopy Files Wizard: Configuration Emulati 🔀	
 Which configuration mode emulation do you want to use? Do not use any emulation. Use existing HardCopy device power up. Use combination of existing HardCopy device power up and 50ms of do 	HardCopy Wizard: Configuration Scheme [pag 🔀
C Use emulation of original target device configuration mode.	Is this device part of a multi-device configuration chain? Yes No Vhich configuration scheme does the target device use? JTAG configuration Passive serial Passive serial Passive parallel asynchronous Passive parallel synchronous Passive parallel Boot from flash



Cancel

Next

Back



N	HardCopy Wizard: Summary	Þ
	When you click Finish, the appropriate HardCopy files will be generated fro information and archived in C:\qdesigns\tutorial\filtref_hardcopy.qar. Send this file to Altera for HardCopy consideration	im the following
	Quartus SOF File identifier: C:\qdesigns\tutorial\filtref.sof 	
	Does the design contain any pre-loaded RAM? No.	
	Question 2 :	



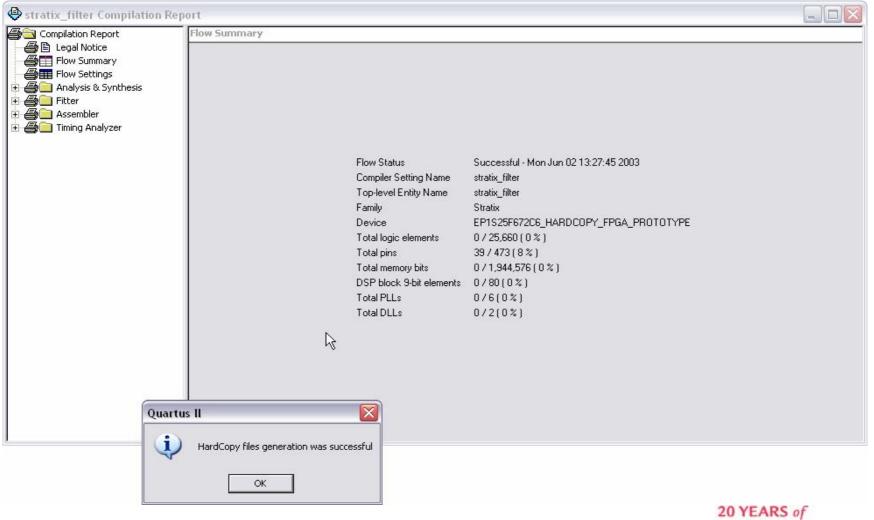
Finish

Cancel

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Next





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HardCopy Generated Files Summary

🗉 stratix_filter_hardcopy - WordPad	
File Edit View Insert Format Help	
い き 日 香 は 株 ※ 階 館 い 🧠	
Quartus II Archive log c:\qdesigns\stratix\s	stratix_filter_hardcopy.qarlog
Archive: c:\qdesigns\stratix\stratix filter hard	icopy.gar
Date: Mon Jun 02 13:28:40 2003	
========== Files Selected: =========	
c:\qdesigns\stratix/hardcopy\stratix filter cksum.c	latasheet
c:\qdesigns\stratix/hardcopy\stratix filter cpld.da	
c:\qdesigns\stratix/hardcopy\stratix filter hcpy.vo	
c:\qdesigns\stratix/hardcopy\stratix filter hcpy v.	
c:\qdesigns\stratix/hardcopy\stratix filter pt hcpy	
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c:\qdesigns\stratix/stratix_filter.hps.txt	
c:\qdesigns\stratix/stratix_filter.pin	
c:\qdesigns\stratix/stratix_filter.psf	
c:\qdesigns\stratix/stratix_filter.sof	
c:\qdesigns\stratix\debug.fsf	
c:\qdesigns\stratix\release.fsf	
c:\qdesigns\stratix\stratix_filter.asm.rpt	
c:\qdesigns\stratix\stratix_filter.csf.rpt	
c:\qdesigns\stratix\stratix_filter.drc.rpt	
c:\qdesigns\stratix\stratix_filter.eda.rpt	
c:\qdesigns\stratix\stratix_filter.fit.rpt	
c:\qdesigns\stratix\stratix_filter.map.rpt	Details Of The File
c:\qdesigns\stratix\stratix_filter.quartus	
c:\qdesigns\stratix\stratix_filter.qws	Listed In Chapter 14
c:\qdesigns\stratix\stratix_filter.ssf	•
c:\qdesigns\stratix\stratix_filter.tan.rpt	Handbook
====== Total: 25 files to archive =======	

All files archived successfully.

Details Of The Files archived in the .qar file are Listed In Chapter 14 of the HardCopy Device Handbook





HardCopy Power Estimation

- In The HardCopy Project Directory, Invoke The Power Calculator As Shown Thru The Menu.
- Upon Running The Power Estimation Command, Quartus II Automatically Sends Information And Configures The HardCopy Power Calculator On Altera's Web Site
- Some Information Will Have To Be Entered Manually. Most information can be changed manually.

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Project Assignments Processing Tools. Wi Add Current File to Project Add/Remove Eiles in Project... Archive Project... Restore Archived Project... Generate Tcl File for Project... HardCopy Optimization Wizard... HardCopy Files Wizard... HardCopy Power Estimation 😘 Locate in Timing Closure Floorplan st Compilation Floorplan hip Editor Opening HardCopy Power Calculator page on Altera web site. Click Help for more information. esign File Sending the following information to HardCopy Power Calculator page: * target device er Focus to Current Entity Ctrl+J * target device package * temperature grade of target device * clock domain fmax Int Focus Entity Ctrl+F * number of flipflops Ctrl+D ted Entity * number of logic elements * number of output and bidirectional pins Ctrl+U t Entity * number of Embedded System Blocks. Manually enter all other relevant information in the HardCopy Power Calculator page, including the following information: Level File in Hierarchy Ctrl+T * average logic element toggle (defaults to 12.5) * average capacitive load (defaults to 10pF) * DC output power * ambient temperature. After entering information in HardCopy Power Calculator page, click Calculate. 20 YEARS of

INNOVATION

HardCopy Power Estimation (continue)



Table 1. De	vice					
Device	Package	Temperature Grade	V _{CCINT}	Total P _{INT} (mW)	Total P ₁₀ (mW)	Total P _{TOTA} (mW)
HC1S25 💌	672 FineLine BGA 💌	C-commercial 💌	1.5	140.81	2.41	143.23

l _{CC} <u>Standby</u> (mA)				
Typical	-	90.0	0	
[Go to Top]	Ca	lculate		

Clock Tree

Global lock Network	É _{MAX} (MHz)	<u>Number of</u> <u>Flip-Flops</u>	ICCINT (mA)	P _{INT} (mW)
1	100.00	50.00	3.64	5.46
2	10.00	8.00	0.18	0.27
з	0.00	0.00	0.00	0.00
4	0.00	0.00	0.00	0.00
5	0.00	0.00	0.00	0.00
6	0.00	0.00	0.00	0.00
7	0.00	0.00	0.00	0.00
8	0.00	0.00	0.00	0.00
9	0.00	0.00	0.00	0.00
10	0.00	0.00	0.00	0.00
11	0.00	0.00	0.00	0.00
12	0.00	0.00	0.00	0.00
13	0.00	0.00	0.00	0.00
14	0.00	0.00	0.00	0.00
15	0.00	0.00	0.00	0.00
16	0.00	0.00	0.00	0.00
		Subtota	3.82	5.73

[Go to Top] Calculate

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HardCopy Stratix Power Calculator - Summary

Calculate << Go back to Step 4

- <u>Clock Tree</u>
 - Global Clock Network
 - <u>Regional Clock Network</u>
 - Fast Regional Clock Network
- Logic Element (LE)
- <u>Digital Signal Processing (DSP) Blocks</u>
- Phase-Locked loops (PLL)
 - o Enhanced Phase-Locked Loops
 - o Fast Phase-Locked Loops
- <u>RAM blocks</u>
 - o M512 Blocks
 - M4K Blocks
 - M-RAM Blocks
- High-Speed Differential Interface (HSDI)
 - o Receiver
 - <u>Transmitter</u>
- General I/O Power Consumption
- Terminator Technology
- <u>Total Power</u>
- <u>Thermal Analysis</u>
 - o <u>Without Heat Sink</u>
 - o With Heat Sink





Designing For HardCopy (Back-Up Slides)



Designing For HardCopy

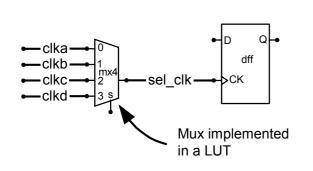
- Guidelines To Permit A Successful FPGA To HardCopy Device Conversion
- Good General Design Practice Guidelines
- Design Assistant Examines The Conformance Of Your Design Against These Design Rules
- Take Corrective Design Actions Based On Feedback From Design Assistant
- Case study

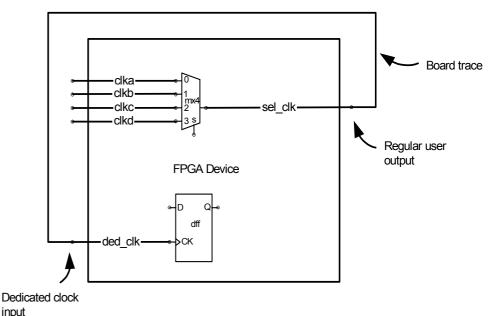




Clocks

 All Clock Signals In A Design Should Be Global Signals Clock Signals That Are Mapped To Regular Logic Can Affect The Performance Of The Design (i.e. Might Not Work)







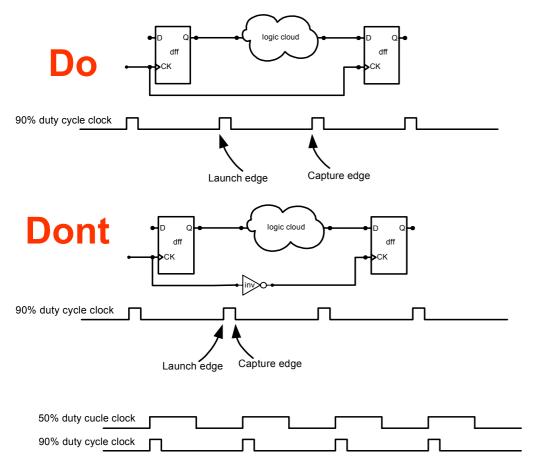
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Better To Do

•Easier STA •Two Extra Pins



Clocks



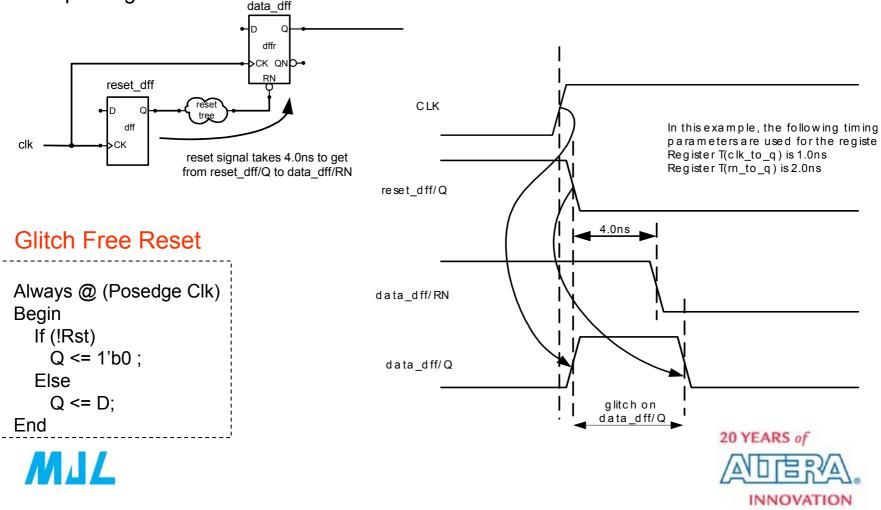
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- Any Time A Circuit Needs To Use Both Edges Of The Clock, The Duty Cycle Has To Be Accurately Described For Proper Static Timing Analysis
- Try To Use Same Edge Clocking To Avoid Warnings By The Design Assistant

Duty Cycle Will Determine Success In Meeting Timing Not Frequency (Probably Not The Intention)



- Reset
- Reset Trees Have Inherent Delays In Them That Might Cause A Glitch On The Output Of Registers If This Presents A Problem In Your Design, Make Reset Part Of Your Input Logic



HardCopy Recommendation 3 Timing Closure

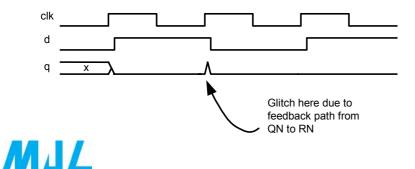
- Minimize Excessive Number Of Loads On Nets. This Will Improve Your Chances Of Meeting Your Design Goals
- If The Two Registers Are Triggered By Clock Edges At The Same Time, A Hold Time Violation May Occur. This Is Only A Design Assistant Info Message





Non-synchronous Design Structure

- A Design Should Not Contain Any Combinatorial Loops These Combinatorial Loops Can Cause Significant Stability And Reliability Problems In A Design
- A Design Should Not Contain Any Combinatorial Loops Where The Output Of A Register Directly Drives One Of Its Own Control Signals



Combinatorial feedback path

