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# Successful High-Speed Board Design

# What Is High Speed?

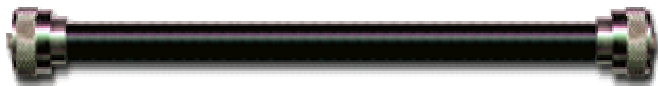
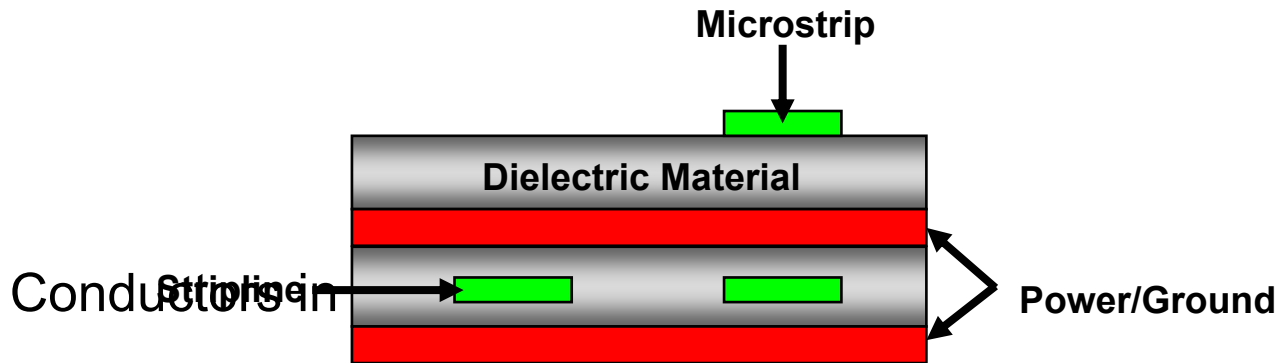
- Definition of High Speed Has Changed with Technology
  - 1990: 50 MHz
  - 1995: 200 MHz
  - 2002: 1.25 – 3.125 Gbps or More
- Faster Systems Require More Attention to Detail

# Agenda

- Ideal Transmission Lines
- Termination
- Lossy Transmission Lines
- Pre-Emphasis & Equalization
- Simulation (Using HyperLynx)
- References
- Summary

# Wires

- Wires in Digital Systems Consist of
  - Traces on PC Boards & Backplanes
    - i.e., Microstrip & Striplines



Coaxial Cable



Tyco VHDM Connectors

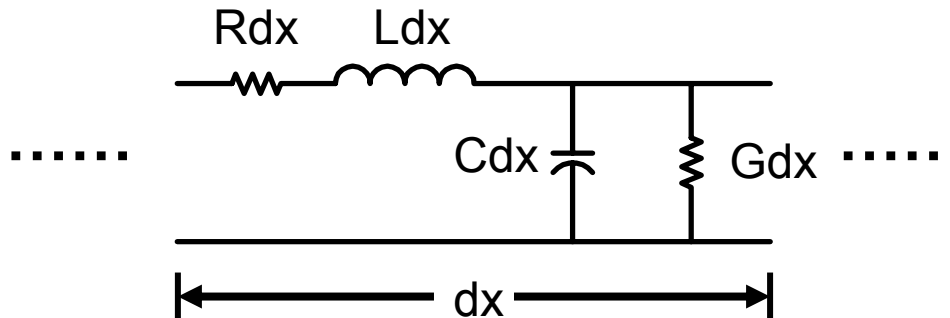
# Wire Model

- Traditional Wire Model - Ideal
  - No Capacitance, Inductance or Resistance



Traditional Wire Representation

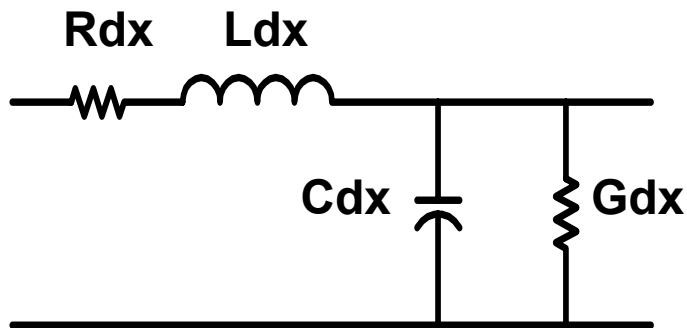
- High-Speed Analysis
  - Model Wire as Infinitesimal Segments of Resistance-Inductance-Conductance-Capacitance (RLGC) Elements



Infinitesimal Segment of a Wire Modeled as RLGC Circuit

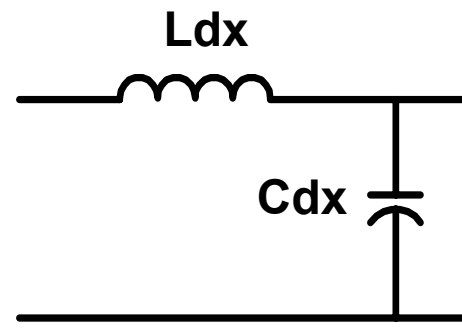
# Lossless Transmission Line Model

- R & G Significantly Small
  - Omitted for First-Order Approximation
  - No Line Losses from Dissipation
- R & G Components of Impedance Significant Only for High-Frequency or Lossy Lines



RLGC Wire Representation

$$Z_o = \left( \frac{R + Ls}{G + Cs} \right)^{1/2}$$



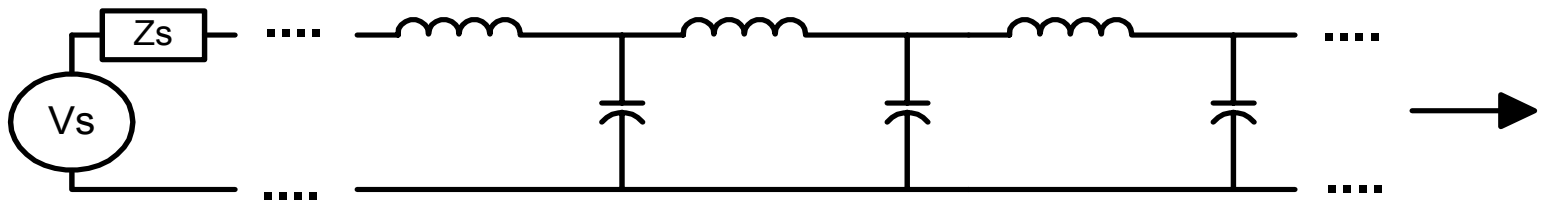
First Order Approximation Wire Representation

$$Z_o = \left( \frac{L}{C} \right)^{1/2}$$

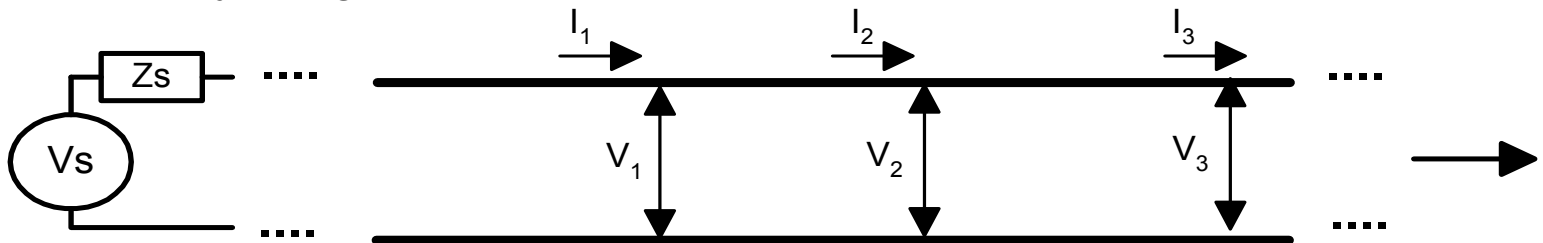
# Characteristic Impedance

- Characteristic Impedance ( $Z_0$ ) of Transmission Line
  - Ratio of Voltage & Current Waves at Any Point of Line

$$Z_0 = \left( \frac{L}{C} \right)^{1/2} = \left( \frac{V}{I} \right)$$



Infinitely Long Representation of a Transmission Line Model



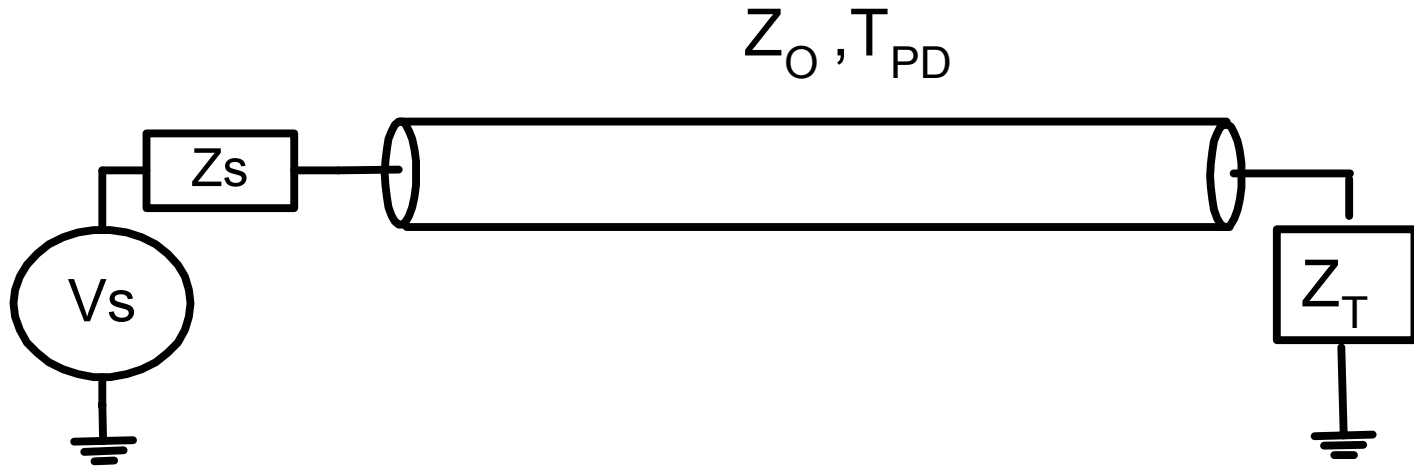
Infinitely Long Representation of a Transmission Impedance



# Transmission Line Representation

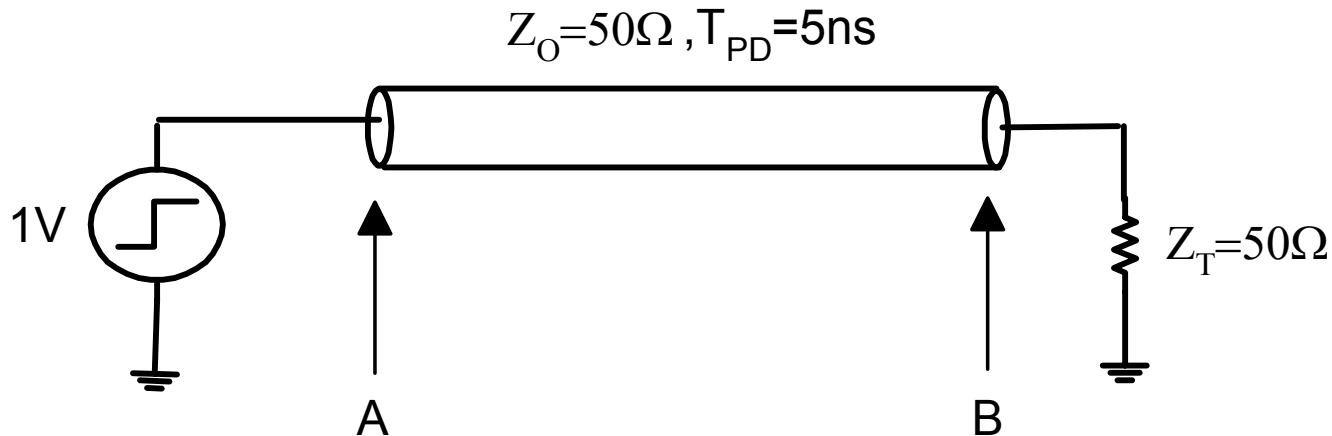
## ■ Transmission Line Characteristics

- Characteristic Impedance,  $Z_0$
- Length (Propagation Delay),  $T_{PD}$



# Transmission Line Basic Rules

- Three Basic Rules for Transmission Line Analysis
  - Waves Propagate on Line
    - Both Directions
  - Waves Reflect Unless Terminated
  - Voltage Is Superposition of Waves



*Later Slides Show Simulation Example*

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# Termination Circuits

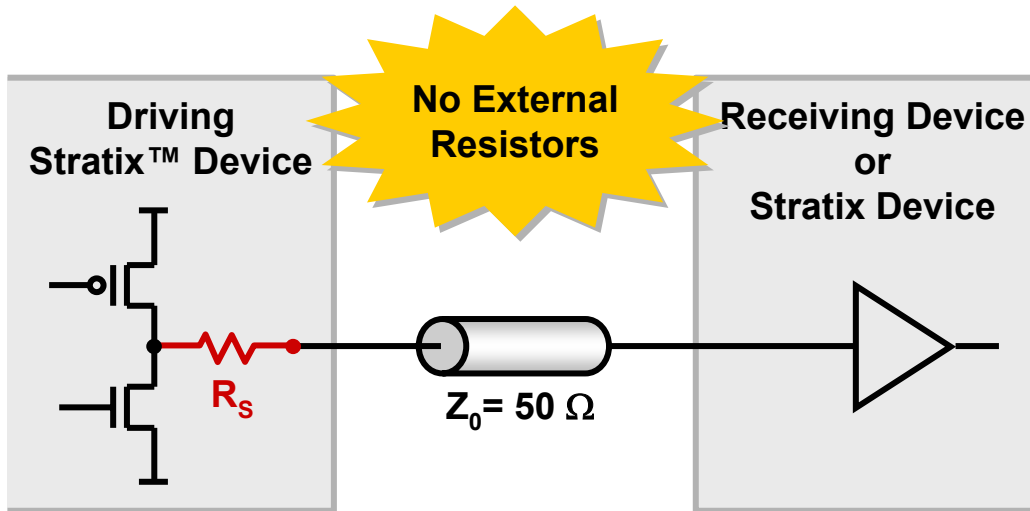
- Many Common Termination Circuits
  - Parallel Termination
  - Series Termination
  - Thevenin Load Termination
  - Active Load Termination
  - Fly-By Termination
  - Differential Termination

# Stratix Terminator Technology

- On-Chip Termination Resistors
  - Dynamically Adjust with Voltage & Temperature
  - Two Reference Resistors Required for Each I/O Bank
- Each I/O Bank is All Parallel or All Series
  - External Resistors Must be Used if Both Series & Parallel Termination Required

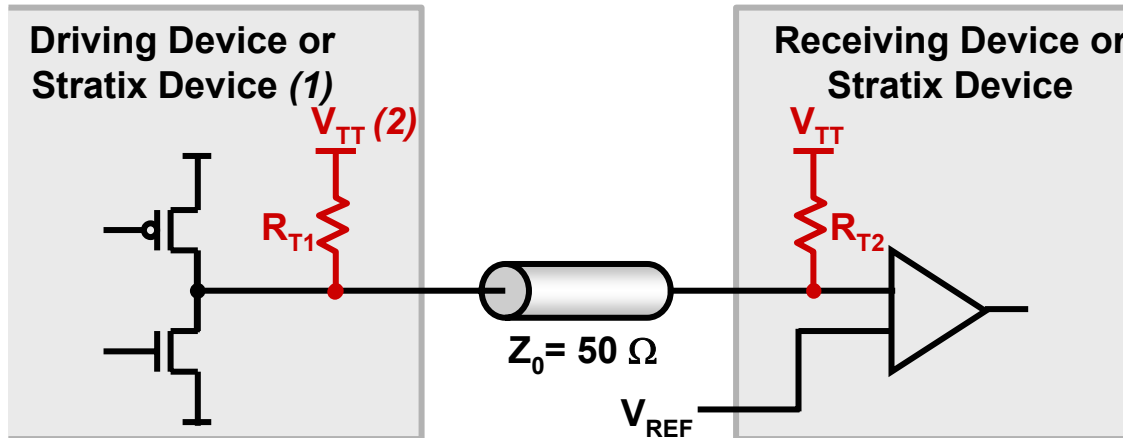
Termination Type	Top & Bottom I/O Banks	Left & Right I/O Banks
Series / Impedance Matching ( $R_s$ )	✓	✓
Parallel ( $R_t$ )	✓	
Differential		✓

# Series Termination & Impedance Matching



I/O Standard	$R_s$
3.3-/2.5-/1.8-V LVTTTL	25 or 50 $\Omega$
3.3-/2.5-/1.8-V LVCMOS	25 or 50 $\Omega$
SSTL-2/-3 Class I	25 $\Omega$
SSTL-2/-3 Class II	25 $\Omega$

# Parallel Termination



(1) HSTL Class II Pin Example

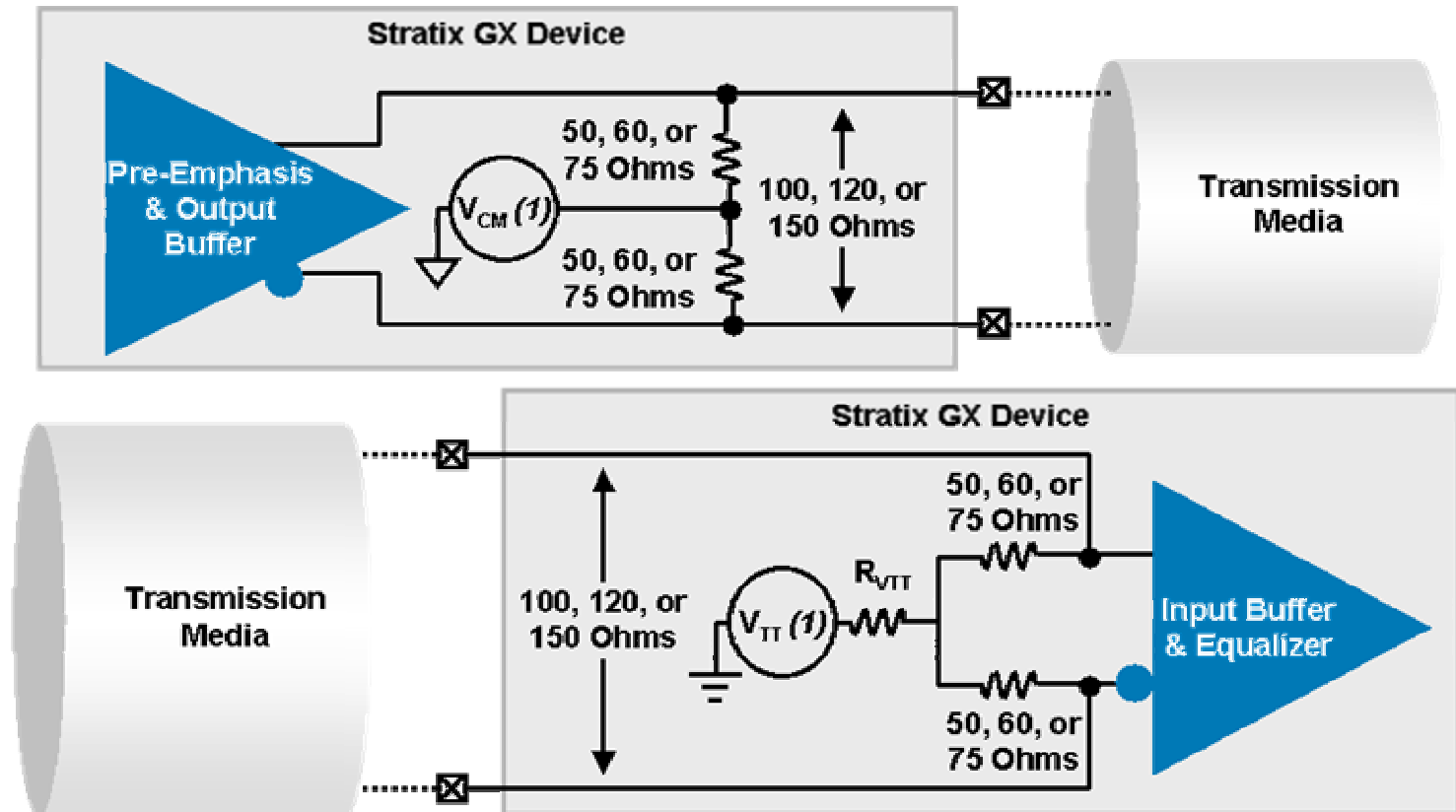
(2) Internally Generated

I/O Standard	$R_{T1}$	$R_{T2}$
SSTL-2/-3 Class I	-	50 $\Omega$
SSTL-2/-3 Class II	50 $\Omega$ (3)	50 $\Omega$
HSTL Class I	-	50 $\Omega$
HSTL Class II	50 $\Omega$	50 $\Omega$
GTL / GTL+	50 $\Omega$	50 $\Omega$
CTT	-	50 $\Omega$

(3) Driver Uses On-Chip Series & External Parallel Termination Resistors

# Stratix GX Differential Termination

- Stratix GX Offers On-Chip Differential Termination
  - Both Transmitter & Receiver





# Agenda

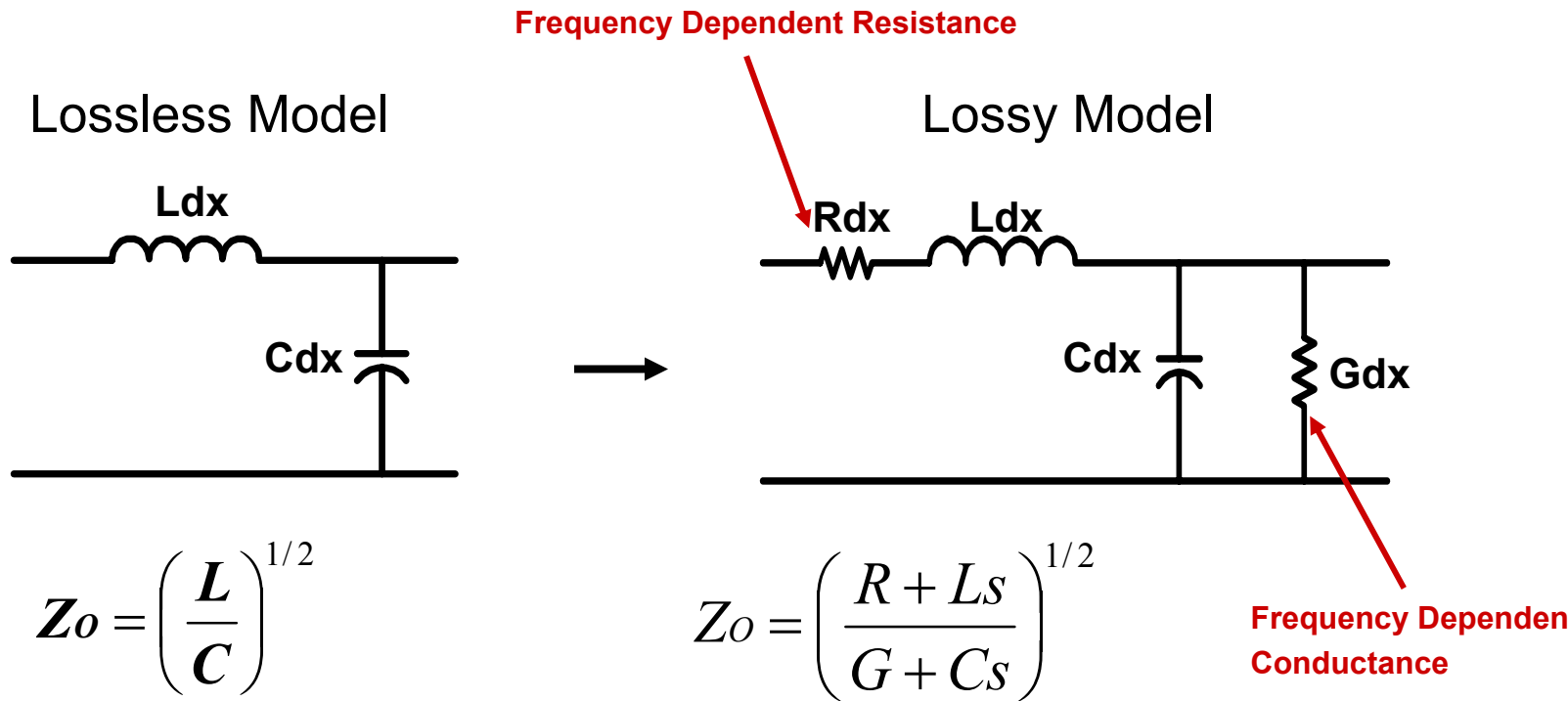
- Transmission Lines
- Termination
- **Lossy Transmission Lines**
- Pre-Emphasis & Equalization
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# Lossy Transmission Lines

- High-Frequency Signals Subject to Losses within Transmission Medium
  - Skin Effect Causes Frequency-Dependent Series Resistance
  - Dielectric Absorption Causes Frequency-Dependent Conductance
- Both Skin Effect & Dielectric Absorption Increase High-Frequency Attenuation

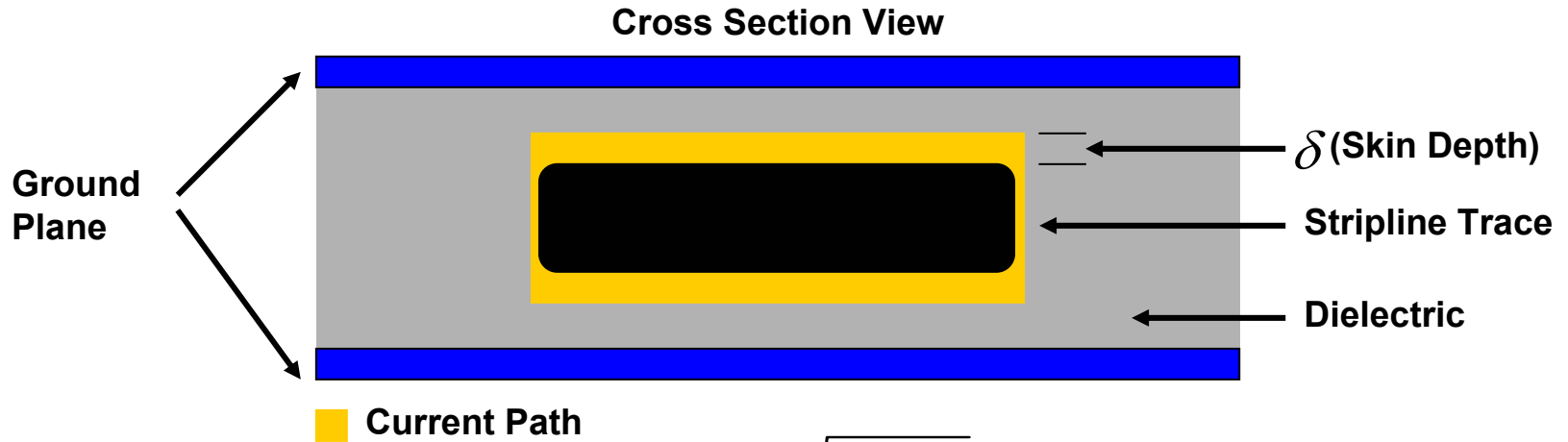
# Lossy Transmission Line Model

- Cannot Omit R & G When Analyzing Lossy Transmission Lines



# Skin Effect

- High-Frequency Current Flows Primarily on Conductor Surface
- Changing Current Distribution Increases Resistance as Function of Frequency



$$\delta = \sqrt{\frac{\rho}{\pi F \mu}}$$

Resistivity

Permeability of Free Space

Frequency

# Dielectric Absorption

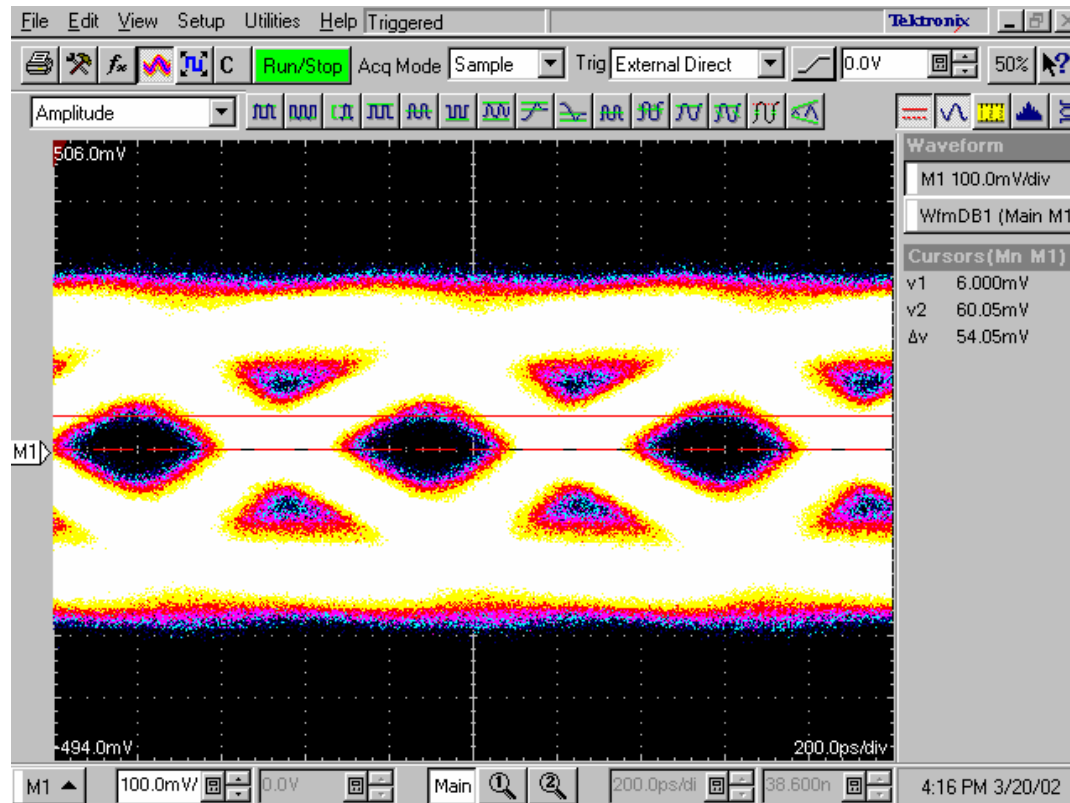
- High-Frequency Signals Excite Insulator Molecules
  - Attenuate Signal
- Dielectric Absorption Often Specified as Loss Tangent  $\tan(\delta)$
- Lower  $\tan(\delta)$  = Less Loss

List of Common Dielectric Material Loss Tangents

Material	$\tan(\delta)$ @1MHz
FR4	0.035
Polyamide	0.025
GETEK	0.010
Teflon	0.001

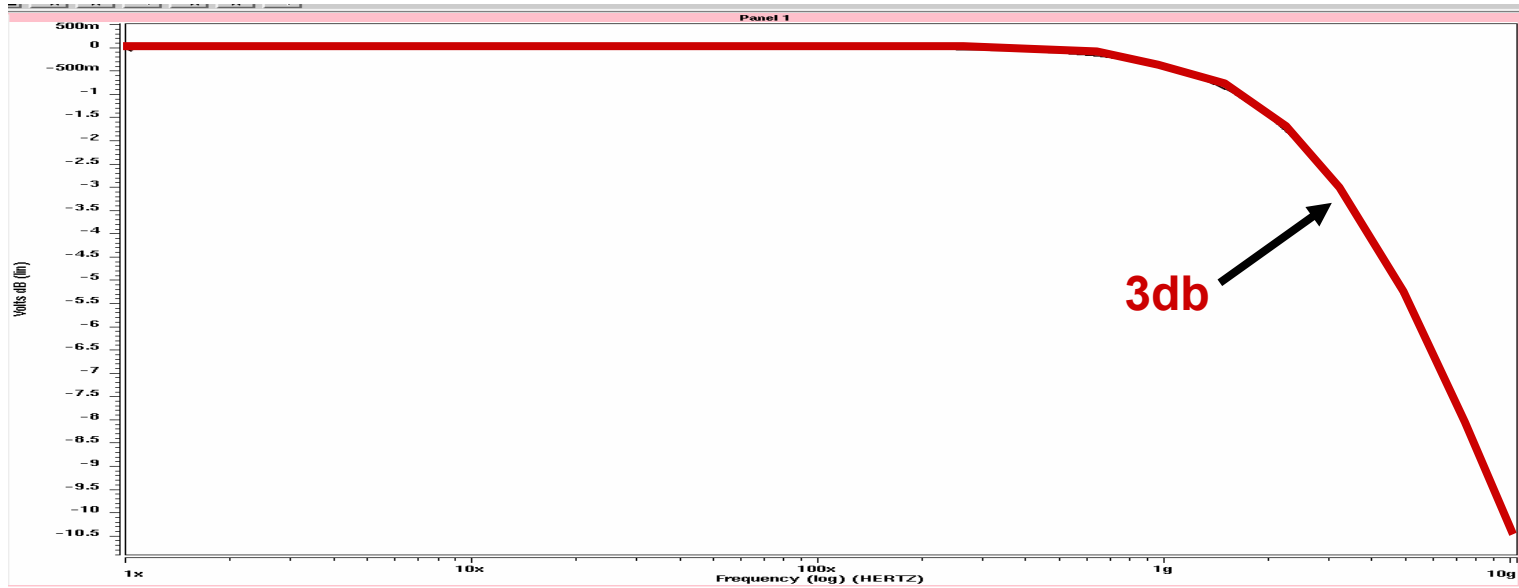
# Why Are Losses Important?

- Transmission Line Losses Attenuate Eye Diagram
  - Reduces Noise Margins



# Effects of Lossy Line

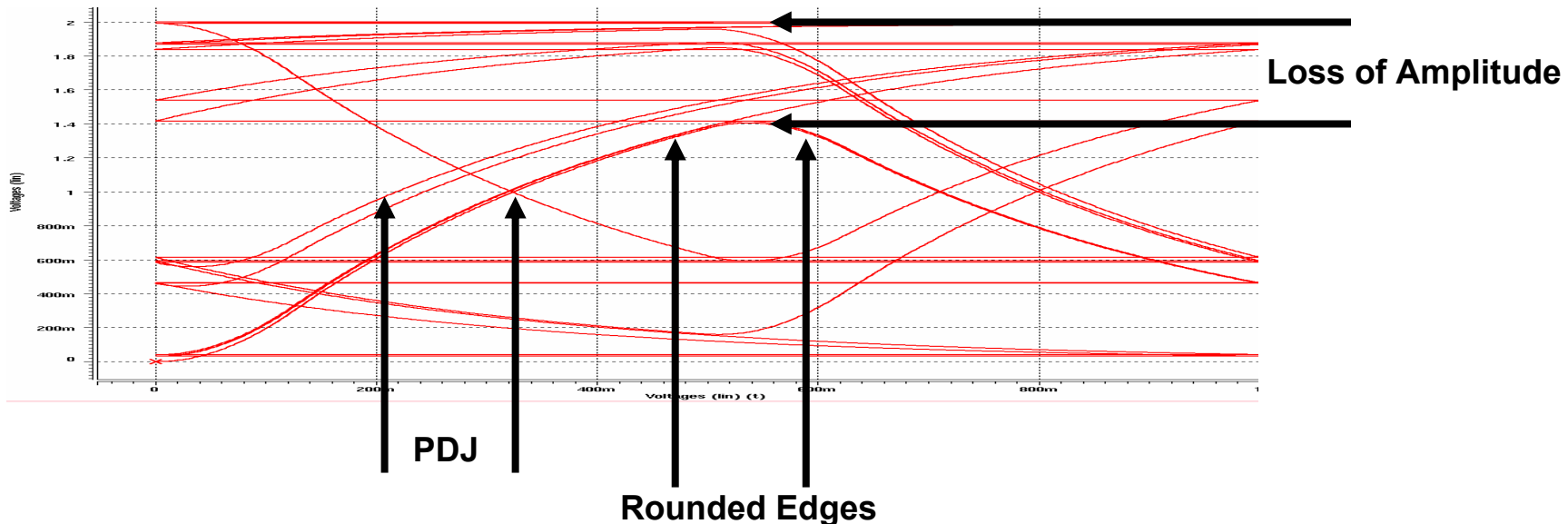
- Effect 1: IR Loss (Frequency Attenuation)
  - Caused By Skin Effect Increasing Resistance for High Frequency Signals
  - Simulate Frequency Response as Low Pass Filter



# Effects of Lossy Line

## ■ Effect 2: Pattern-Dependent Jitter (PDJ)

- Due to Intersymbol Interference (ISI)
- Rise & Fall Times Affected by Data Sequence





# Agenda

- Transmission Lines
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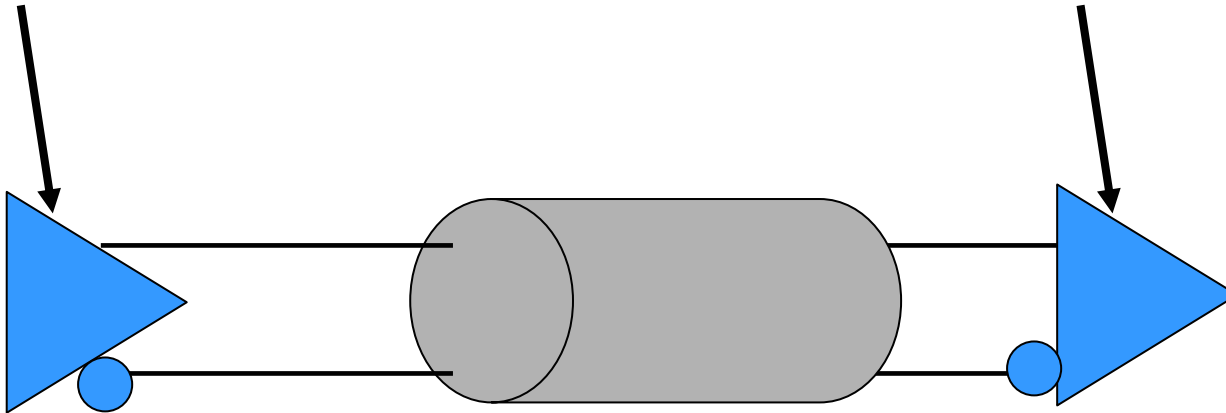
# Compensate for Lossy Line

- Compensate for Losses, Boost High-Frequency Components
- Increasing Overall Signaling Level Causes Negative Effects
  - Increases Proportional Noise
  - Increases Pattern-Dependent Jitter
  - Increases Power Consumption

# Pre-Emphasis & Equalization

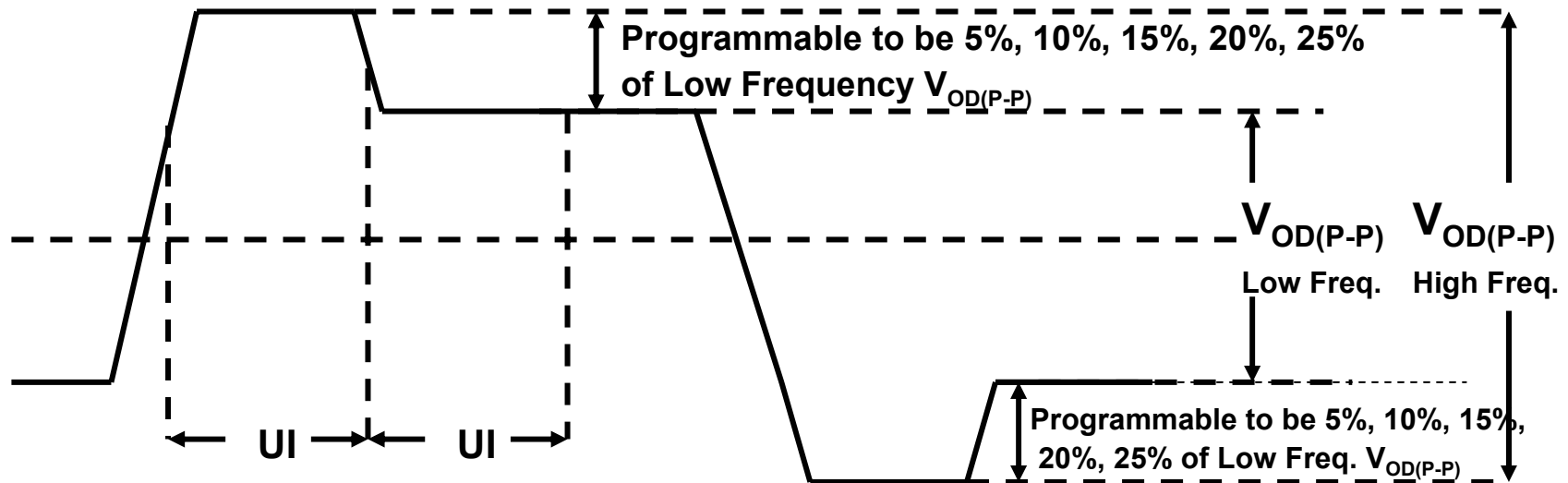
Driver Uses Pre-Emphasis

Receiver Uses Equalization



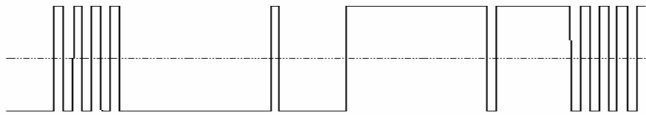
# Pre-Emphasis Theory

- Reduce PDJ, Increase (Pre-Emphasize) High-Frequency Components
  - When Signal Switches, Increase Differential Swing
  - When Run Length Exceeds One, Signal Is De-Emphasized to Lower Voltage Level

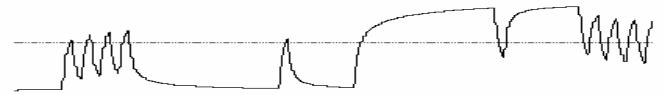


# Pre-Emphasis Example 1

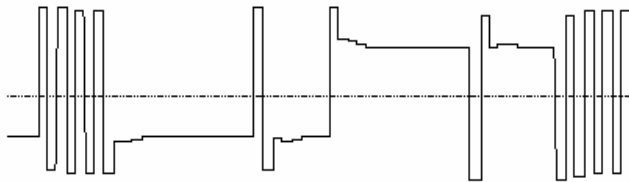
Transmitter with  
No Pre-Emphasis



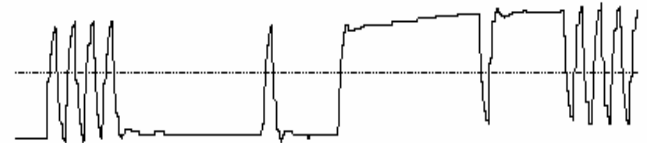
Receiver with No  
Pre-Emphasis



Transmitter with  
Pre-Emphasis



Receiver with  
Pre-Emphasis

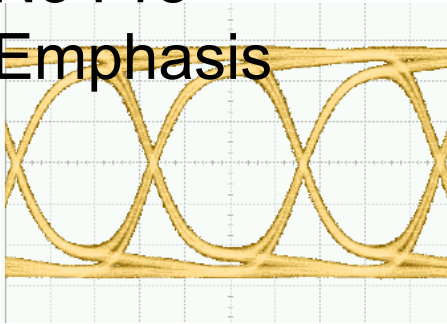


Signal Transmitted over 1-m, 5-mil Stripline

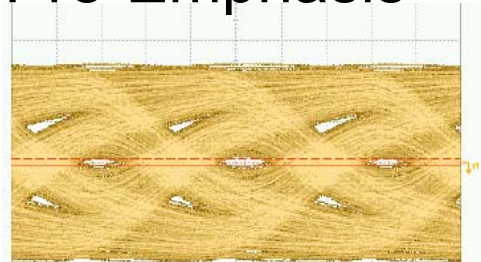
Digital Systems Engineering, William J. Dally & John W. Poulton, Pg 365

# Pre-Emphasis Example 2

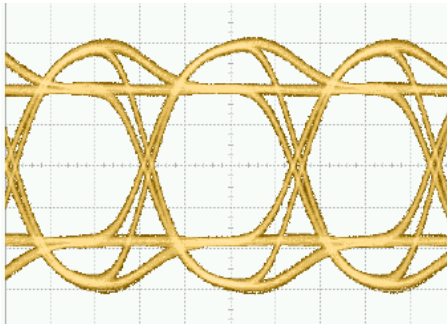
Transmitter with  
No Pre-  
Emphasis



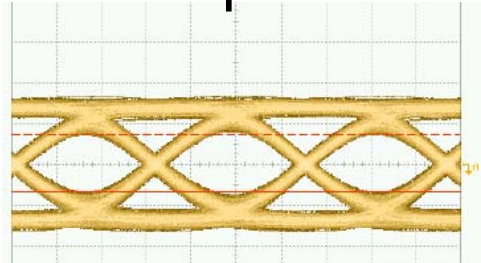
Receiver with No  
Pre-Emphasis



Transmitter with  
Pre-Emphasis



Receiver with  
Pre-Emphasis



# Stratix GX Programmable Pre-Emphasis

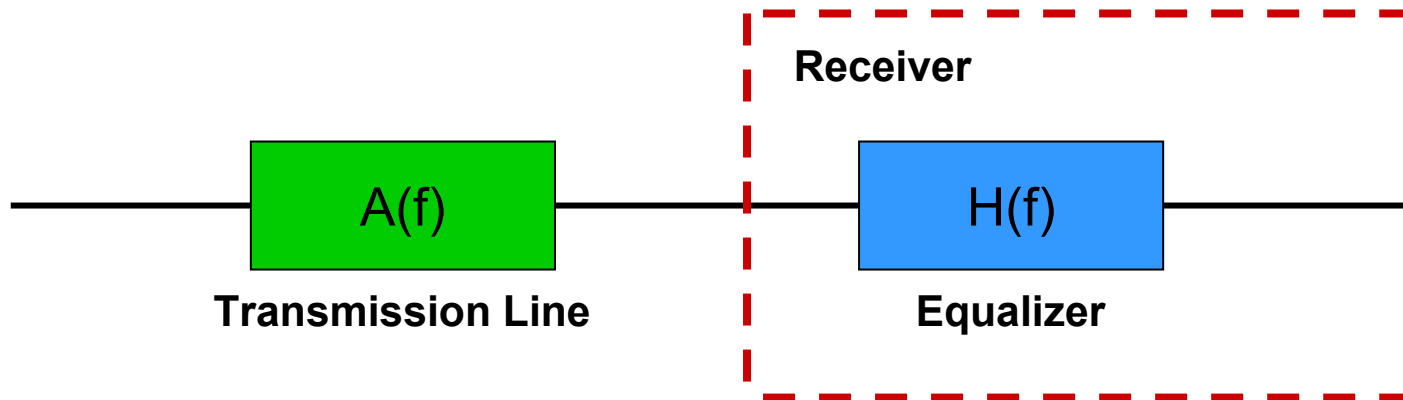
- Support for 0% to 25% Pre-Emphasis on Transmitter Channels
  - Maximum Limit for  $V_{OD(\text{peak-to-peak})}$  Is 1,600 mV

Original VOD	$V_{OD}$ with Pre-Emphasis (1)				
	5%	10%	15%	20%	25%
400	420	440	460	480	500
480	504	528	552	576	600
600	630	660	690	720	750
800	840	880	920	960	1000
960	1008	1056	1104	1152	1200
1,000	1050	1100	1150	1200	1250
1,200	1260	1320	1380	1440	1500
1,400	1470	1540			
1,440	1512	1584			
1,500	1575				
1,600					

(1) Calculated as a Percentage of Original  $V_{OD}$  Setting

# Programmable Equalization

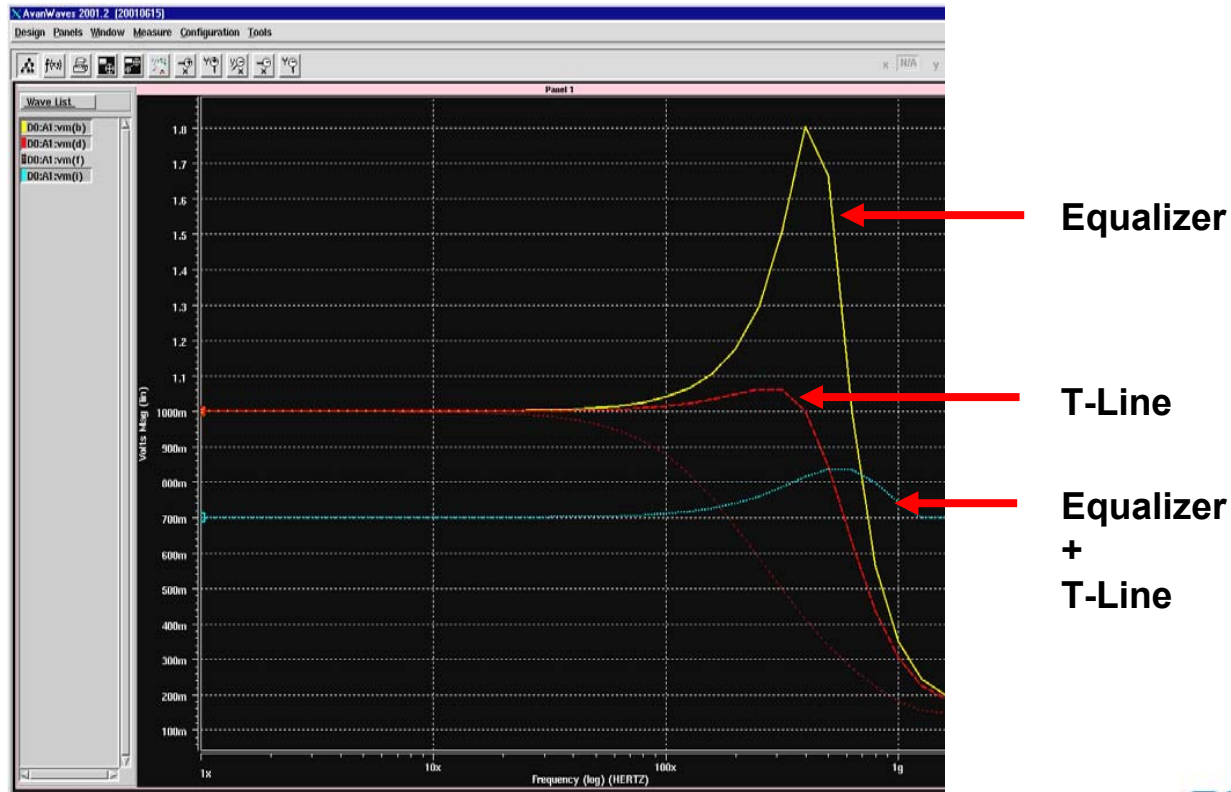
- Receiver Uses Programmable Equalization to Boost High-Frequency Gain
  - Negates Effect of High-Frequency Losses
- Stratix GX Equalizer Compensates for 20" or 40" of FR4 Trace
  - Boosts Signals Up to 9 dB





# Equalization Effect

- Equalizer Successfully Compensates for Transmission Line Attenuation
- Blue Line Shows Overall Flat Response

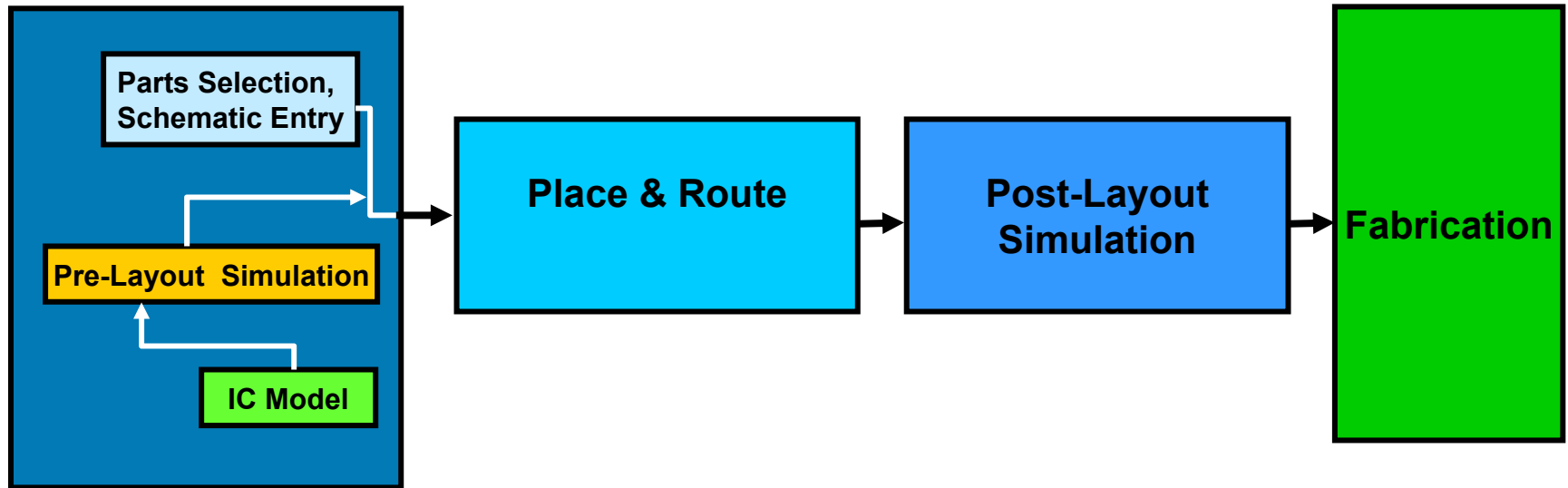


# Agenda

- Transmission Lines
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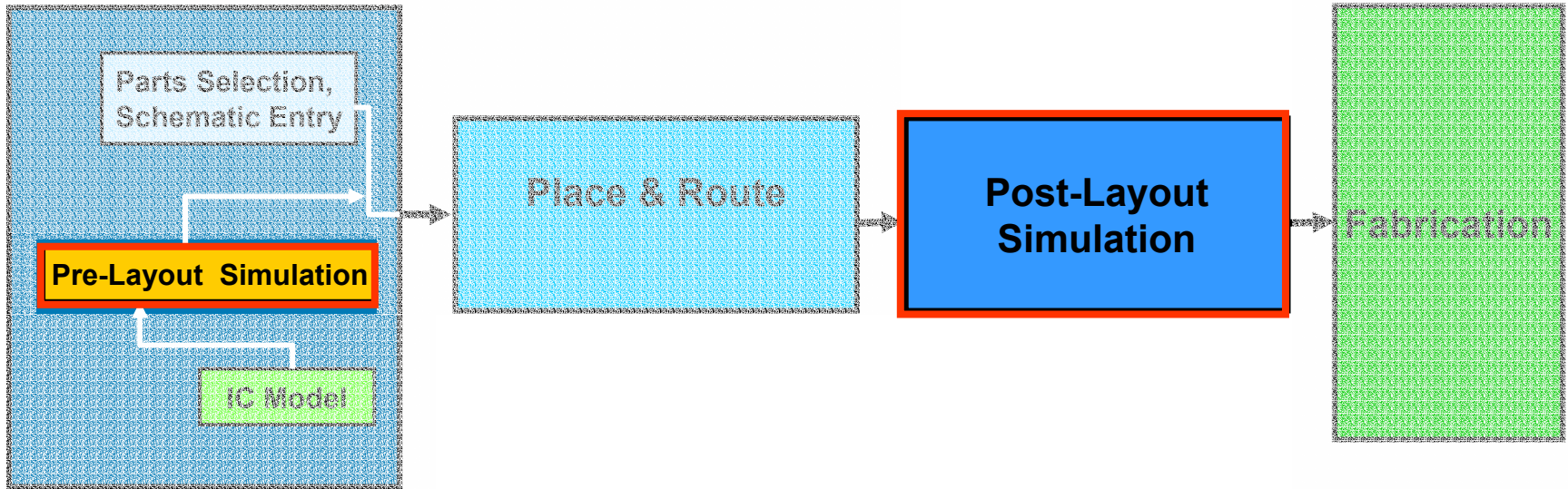
# PCB Design Flow

## Pre-Layout



# PCB Design Flow

## Pre-Layout



# Two Types of Simulation

## Pre-Layout

The collage displays several HyperLynx windows during the pre-layout phase:

- Edit Stackup:** Shows a 4-layer stackup: 1 TOP (green), 2 GND (yellow), 3 VCC (blue), 4 BOTTOM (red). It notes that impedances are computed from the test trace width and that no errors were found.
- Transmission Line:** Shows a cross-section of a microstrip line on a dielectric substrate with parameters like Length, Plating Thickness, Conductor Thickness, Width, Dielectric Height, and Dielectric Constant.
- Vertical 1 Wdv offset:** A graph showing a signal waveform with a cursor at 6.52 ns.
- Vertical 1 Wdv offset:** Another graph showing a signal waveform with a cursor at 5.1 ns.
- BoardSim:** A detailed view of the PCB layout with various components and traces.

## Post-Layout

The BoardSim window shows a detailed post-layout simulation of the PCB. It features a complex network of traces, components, and vias, with various colors used to represent different signal paths and simulation results. The interface includes standard software menus and toolbars.

# Pre-Layout Simulation

- Examine Stackup of 4-Layer Board
- Tool Calculates Impedance

**Edit Stackup**

Note: Impedances shown below are computed from the test trace width shown in the Edit Selected Layer dialog.  
No errors found in stackup.

Layer	Type	Properties
1	TOP	Sig 1.00 oz, Z0=50.4 ohms Diel 8.00 mils
2	GND	Plane 1.00 oz Diel 40.00 mils
3	VCC	Plane 1.00 oz Diel 8.00 mils
4	BOTTOM	Sig 1.00 oz, Z0=50.4 ohms

Total PCB thickness: 61.40 mils

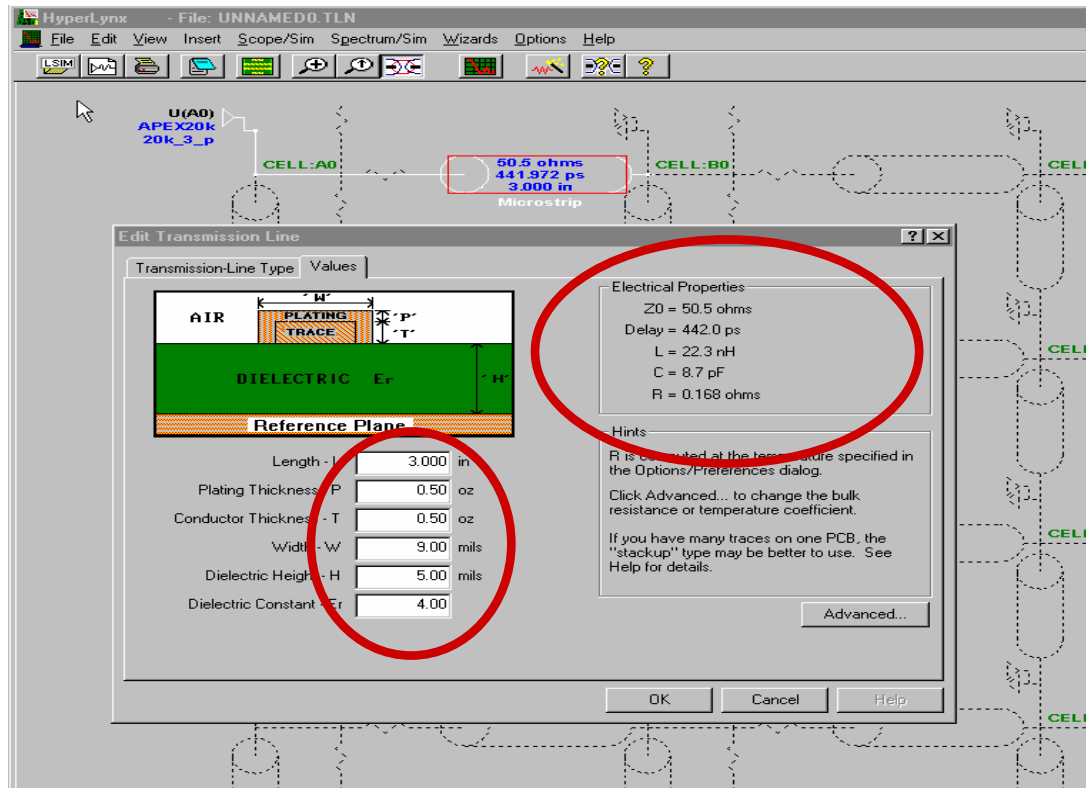
PCB Fabrication Compensation  
 Enable compensation  
Usually disabled (see Help)

Hints  
Select a layer by clicking on it.  
To move a layer, drag it with the mouse.

Buttons: Edit Selected Layer..., Delete Selected Layer, Dielectric Add Layer ^, Signal Add Layer v, Plane Add Layer v, View Stackup Wizard..., Measurement Units..., Copy to Clip, Print..., OK, Cancel, Help

# Pre-Layout Simulation

- Determine Delay, L, C & R Values from Stackup
- Find New Electrical Parameters after Changing Dimensions
  - Microstrip vs. Stripline



# Pre-Layout Simulation

- With New Length, Tool Reports New Electrical Properties

The screenshot shows the HyperLynx software interface. The main window displays a PCB layout with a transmission line simulation window open. The simulation window, titled "Edit Transmission Line", shows the following parameters:

Parameter	Value
Length	6.000 in
Plating Thickness - P	0.50 oz
Conductor Thickness - T	0.50 oz
Width - W	9.00 mils
Dielectric Height - H	5.00 mils
Dielectric Constant - Er	4.00

The "Electrical Properties" section of the window shows the following values:

Property	Value
Z0	50.5 ohms
Delay	883.9 ps
L	1.17 nH
C	17.5 pF
R	0.335 ohms

The "Hints" section provides additional information:

R is computed at the temperature specified in the Options/Preferences dialog.

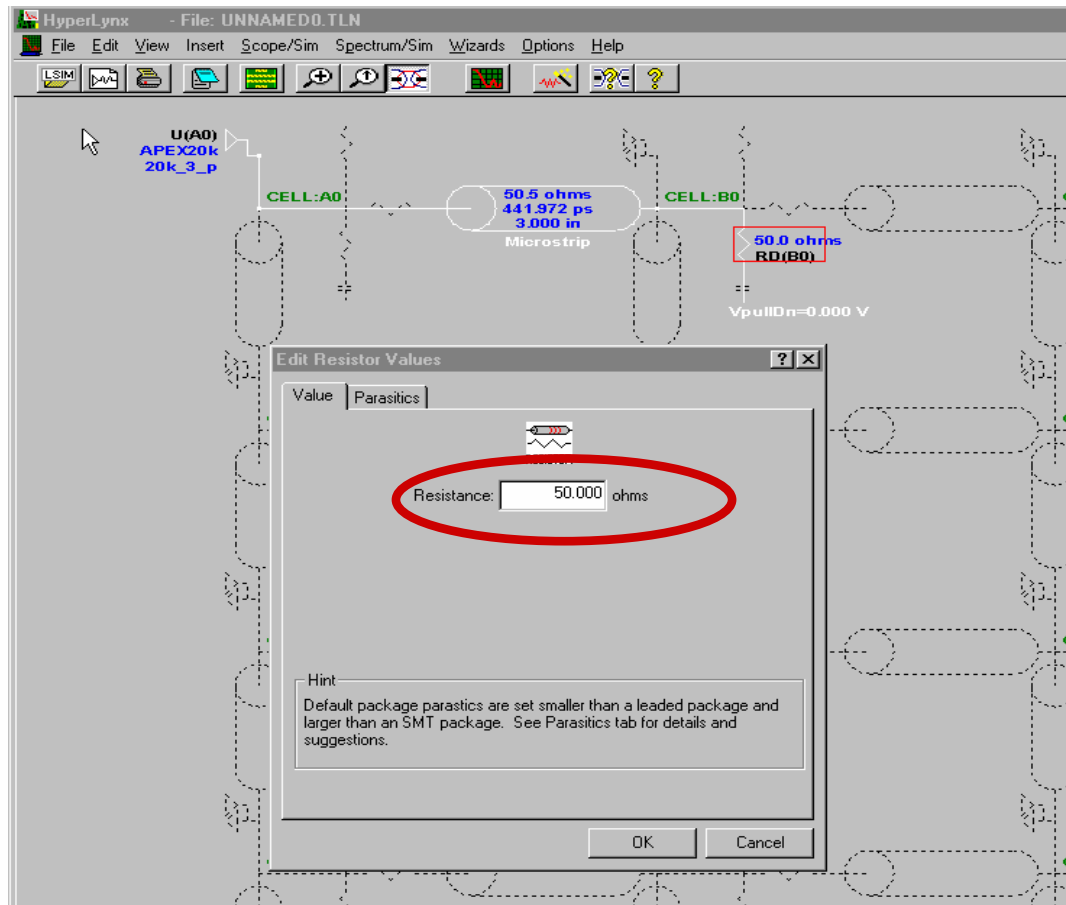
Click Advanced... to change the bulk resistance or temperature coefficient.

If you have many traces on one PCB, the "stackup" type may be better to use. See Help for details.



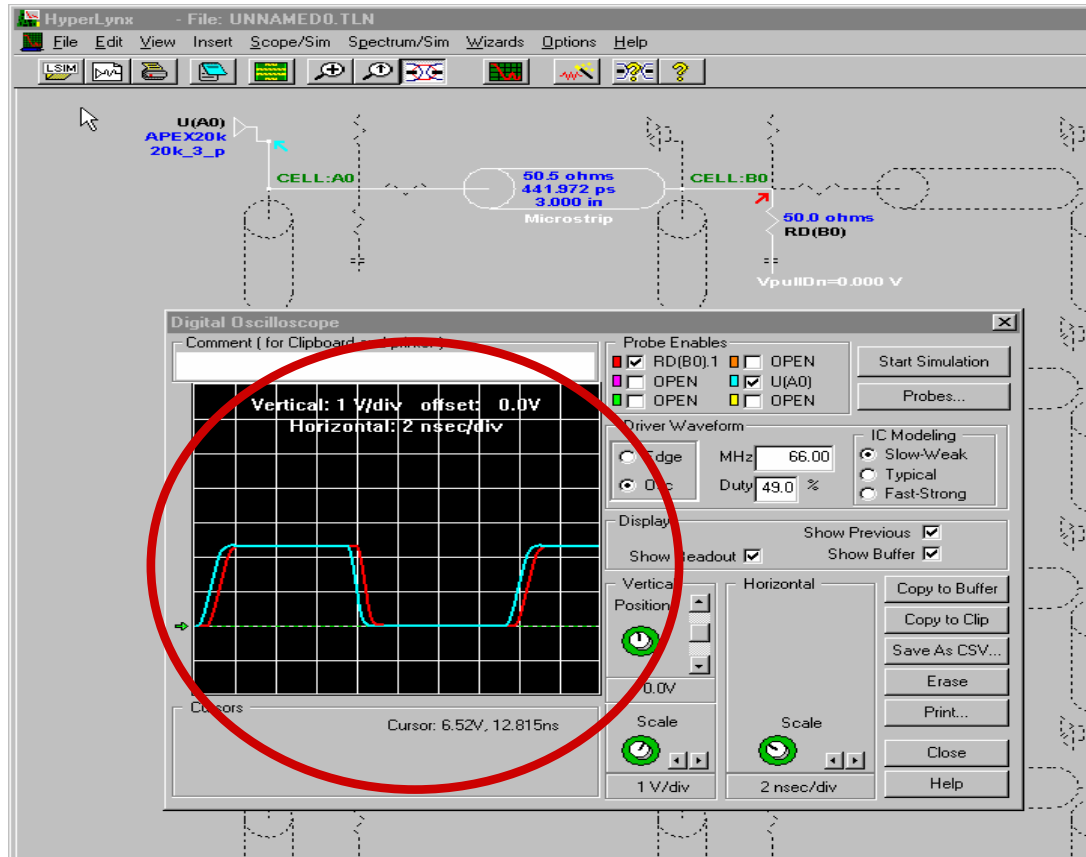
# Pre-Layout Simulation

- Set 50-Ω Termination Resistor for 50-Ω Impedance Board



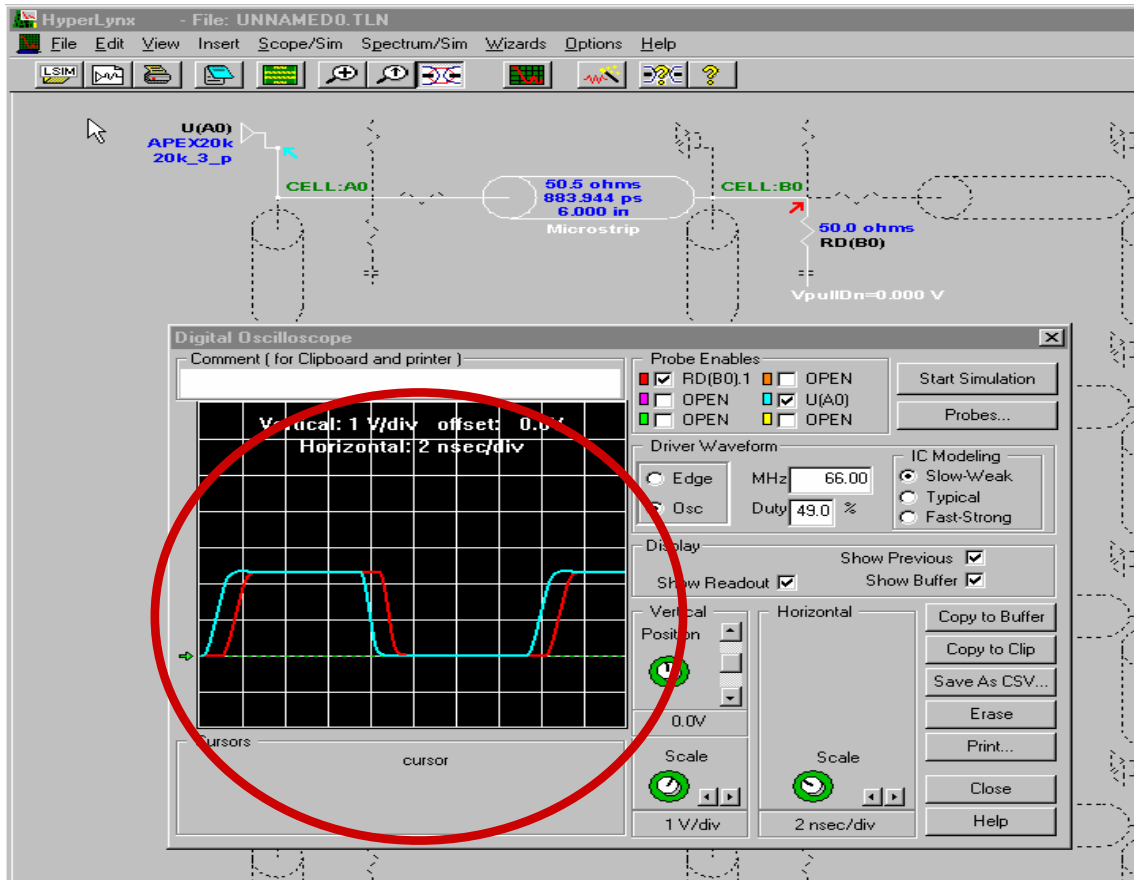
# Pre-Layout Simulation

- Examine Simulation Waveform Output
- Blue & Red Traces Show Different Probe Points



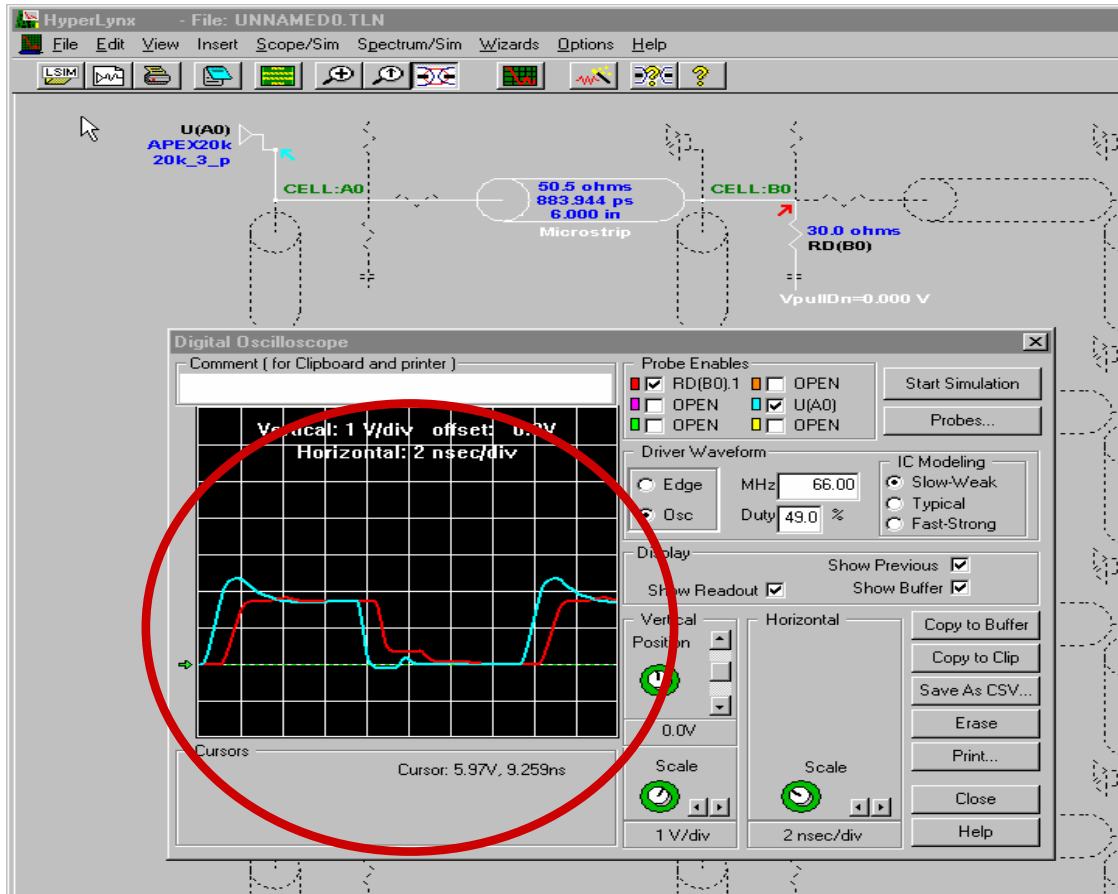
# Pre-Layout Simulation

- Different Line Length Causes Different Delay



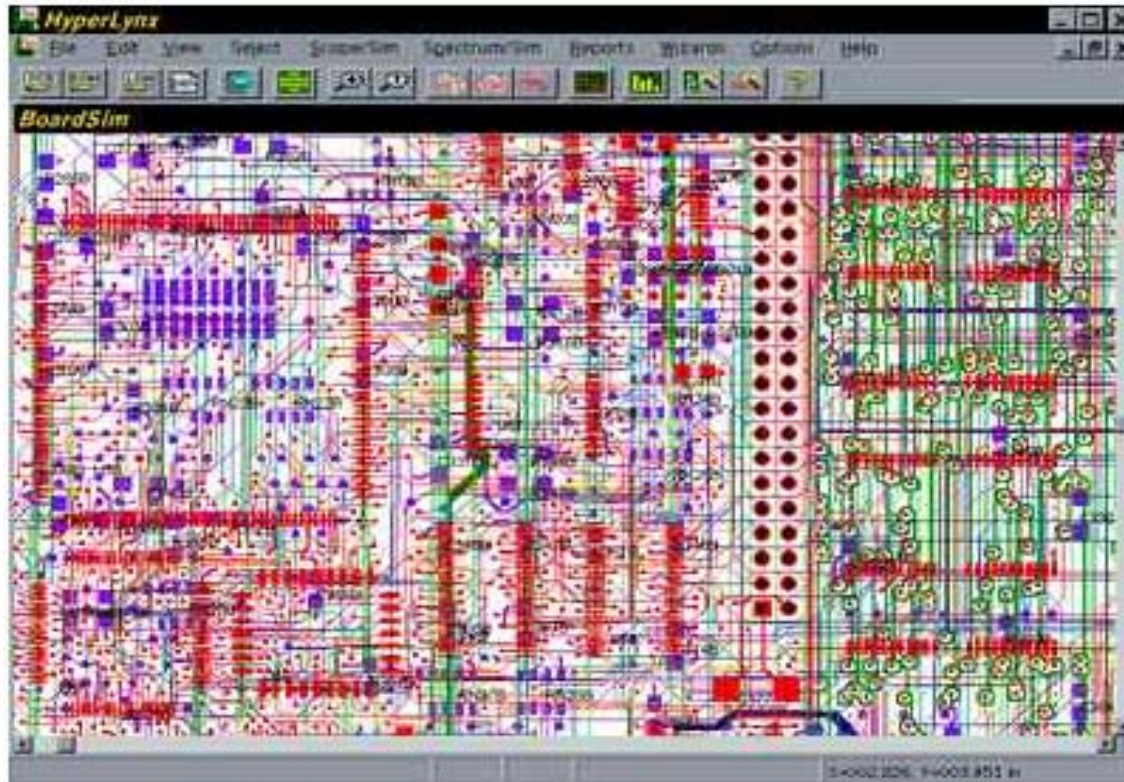
# Pre-Layout Simulation

- 30-Ω Termination Resistor Causes Signal Integrity Issues



# Post-Layout Simulation

- Pull Board Layout into Simulation Tool
- Can Simulate Based on Exact Layout



# Altera Simulation Tools

- Altera Provides IBIS Models on [www.altera.com](http://www.altera.com)
- Encrypted Spice Models Available by Request

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# References

- H. Johnson & M. Graham, High Speed Board Design, Prentice Hall, Inc., 1993
- Stephen Hall, Garrett Hall, & James McCall, High-Speed Digital System Design, John Wiley & Sons, Inc., 2000
- William J. Dally and John W. Poulton, Digital Systems Engineering, Cambridge University Press, 1998
- Altera Application Note 224: High-Speed Board Layout Guidelines



# Summary

- Keys to Success with High-Speed Board Design
  - Understanding Basic Theory
  - Considering Signaling Issues During Design
  - Maintaining Good Communication with Layout Engineer
  - Using Published Guidelines
  - Simulating Design before & after Layout
  - Using Device Features to Ensure High Signal Quality