ChipEditor v5.0
User's Guide

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Introduction

Using ChipEditor

ChipEditor is a graphical application for viewing and placing I/O and logic macros. This tool is particularly useful when you need maximum control over your design placement.

ChipEditor supports the following families: ACT1, ACT2, ACT3, DX, MX, SX, SX-A, and eX families. For all other families, use ChipPlanner.

Use ChipEditor to:

- View macro placements made during layout
- Place, unplace, or move macros
- Fix I/O macro placements
- View net connections using a ratsnest, minimum spanning tree, or route view
- View architectural boundaries
- View and edit silicon features, such as I/O banks
- Cross probe with Silicon Explorer to select probes
- View placement and routing of paths when used with Timer

Starting, Committing, and Exiting

Starting and Exiting ChipEditor

To start ChipEditor:

1. If you have not done so, Compile your design.
2. From the **Tools** menu, click **ChipEditor.** ChipEditor starts in a separate window.

Tip: You can also start ChipEditor by clicking ChipEditor in the Designer design flow window

Exiting ChipEditor:

From the File menu, click Exit. If you haven't committed your changes, you will be asked if you want to commit your changes.

Committing

Changes made are not permanent until you use the Commit command. The Commit command saves your changes to your design session. Changes are not reversible. To permanently save your changes, you must save your design in Designer.

To commit your changes:

1. From the **File** menu, click **Commit**.

Logic Assignment

Manually assigning logic is an optional methodology to help you improve the performance and density of your design.

Assigning and unassigning logic using ChipEditor

You do not need to manually assign logic in your design. However, should you have specific design requirements, ChipEditor and ChipPlanner allow you to have maximum control over your design.

To assign logic using ChipEditor:

1. Select the logic in the Unassigned list box.
2. Drag the logic to the desired location in the ChipEditor Window.

   If the logic placement is valid, the logic is assigned. To remove the placement, from the **Edit** menu, click **Undo**.

   Error messages in the status bar notify you about invalid placement attempts. Choose Extended Error Messages from the Help menu for more details on a specific error message. If you want to ensure that the logic is not moved during layout, you must Lock the logic assignment and commit your changes when exiting ChipEditor.

   Note: Assigning logic to a location that already has logic unassigns the previously assigned logic, even if its assignment was locked.

To assign multiple logic macros:

1. While holding down the CTRL or SHIFT key, select the logic in the order you want it placed.
2. From the **Edit** menu, click **Assign**.
3. One by one, select the desired location. The macros are placed in the order selected.

To unassign logic:

1. Select the logic.
2. From the **Edit** menu, click **Unassign.**

To unassign multiple logic macros:

1. Hold down the CTRL or SHIFT key and select the logic you want to unplace. To select all logic, choose **Select All** from the **Edit** menu.
2. From the **Edit** menu, click **Unassign**.

Moving logic

You can move logic that was assigned manually or automatically during Layout.

To move logic:

1. Select the logic.
2. Drag the logic to the new location.

Tip: To remove the placement, from the Edit menu, click Undo.

Locking logic

Locked logic is not moved during Layout. Locked logic only becomes permanent if you commit the changes to your design before exiting.

To lock macros:

1. Select the macro to lock. To select multiple macros, hold the CTRL key and select multiple macros with your mouse. To select all macros, choose Select All from the Edit menu.
2. From the **Edit** menu, click **Lock**.
3. From the **File** menu, click **Commit** to make the changes permanent and update your .adb file.

To unlock a macro:

1. Select the macro. To select multiple macros, hold the CTRL key and select multiple macros with your mouse. To select all macros, from the **Edit** menu, click **Select All**.
2. From the **Edit** menu, click **Unlock**.

Displaying Resources

Ratsnest

The ratsnest view displays net connectivity between placed logic macros by connecting lines from the output pins to all input pins. Use the ratsnest to understand how logic macros are connected to each other. The ratsnest view is activated by default, showing all input and output nets for the selected macro.

Turn the Ratsnest view on or off by clicking the Ratsnest toolbar button.

Route view

The route view displays a representation of the actual routes used to connect placed macros. This feature helps show the general location of routing segments used by the design.

To activate the route view in ChipEditor:

1. Complete Layout. To display routes, Layout must be completed before running ChipEditor.
2. From the **Nets** menu, choose **input**, **output**, or **both** or click the corresponding Net toolbar icon.
3. From the **Nets** menu, choose Display Algorithm Routes or click the routes icon in the toolbar.
4. Select the placed macro in the ChipView window or Placed list box. Select multiple macros by holding down the CTRL key.

Note: If a macro is moved or unplaced, then the nets connected to that macro will be displayed using a ratsnest.

Clusters and SuperClusters

A cluster is a group of logic elements. The type of elements that make up the cluster is determined by the device type.

A super cluster is at least 2 clusters (SX) or 2 clusters and a buffer (Axcelerator). Modules in a cluster can be connected by fast or direct connects.

Use these areas as guides to ensure that the nets are fast/direct connect for implementation. Nets that connect within a rectangle can be implemented as fast or direct connects, depending on availability. For details about fast connects and direct connects, please see the Actel FPGA Databook.

Note: This feature is only available for the SX, SX-A, eX, and Axcelerator families.

To view clusters or super clusters in ChipEditor:

1. From the **View** menu, select **Static Objects** and click **Cluster or SuperCluster**. The cluster areas appear in the ChipView window.

Locating a net by name

To locate a net by name in ChipEditor:

1. From the **Nets** menu, click **Select Net**.
2. Enter Net name and click **Find**. The net is highlighted in the ChipView window.

Cross-probing with Other Tools

Using ChipEditor with Silicon Explorer

Use ChipEditor to select probes for Silicon Explorer. To use ChipEditor with Silicon Explorer, you must have installed and be familiar with Silicon Explorer.

To select probes using ChipEditor:

1. Open Silicon Explorer.
2. Load the probe file of the current design.
3. Start ChipEditor.
4. Synchronize data. Click the R (Re-sync) button in ChipEditor's toolbar. When completed, the A and B buttons in the toolbar are activated.
5. Select a module in ChipEditor.
6. Click the A button in ChipEditor's toolbar to assign the selected module's output to probe A in Silicon Explorer.
7. Select another module in ChipEditor.
8. Click the B button in ChipEditor's toolbar to assign the selected module's output to probe B in Silicon Explorer.
9. From Silicon Explorer, click the Acquire toolbar button. Waveforms are displayed in Silicon Explorer.

Using ChipEditor with Timer

Use ChipEditor and Timer together to view place-and-route of paths in ChipEditor.

To view paths:

1. Open Timer and ChipEditor from Designer.
2. In **Timer**, click the **Paths** tab.

3. Select a Path set in the path set grid. Paths within that set are displayed below in the path grid.
4. Select the path you wish to expand in the lower path grid.
5. Expand the path by double-clicking on the path, or in the **Edit** menu, click **Expand Path**. The Expanded Paths window opens and displays a path in the Expanded Paths Grid and a graphical representation of the path in the Chart Window. The Expanded Paths grid shows all delay components for the selected path (Instance, Net, Macro, Delay, Type, Total Delay and Fanout details). For Delay, (r) stands for rising edge and (f) for falling edge.
6. Anything selected in the Expanded Paths grid or Graph window is reflected in both windows. Selecting the path number in the Expanded Paths grid highlights the entire path in the Chart window.
    - Selecting an instance, net, or macro in the Expanded Paths grid highlights that selection in the Chart window.
    - Selecting a logic macro in the Chart window, highlights all instances of the macro in the Expanded Paths grid.
    - Toggle the Graph Window on and off by clicking Graph Window from the Window menu. Use the View command menu to Zoom in and out. In the Graph window, dragging the mouse downward and to the left will zoom fit. Dragging downward and to the right drags out a zoom in area.
    - In some cases, long instance names may overlap and be difficult to read in the Graph window. This problem can be solved by moving the module. To move the module, select the module and while holding down the Shift key, click and drag the module to another location.
7. Select a module or net in the Expanded Paths dialog box. The module or net is shown in ChipEditor.

Using the ChipEditor Interface

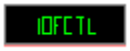
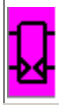
ChipView Window

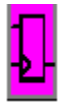
The ChipEditor ChipView window displays logic modules and placed macros. When you select a macro in the ChipView window, the macro location is highlighted in the World View window and the macro name is selected in the Placed list box.

Colors and Symbols Used in ChipEditor

Colors and symbols are used to differentiate the I/O and logic macros in the ChipView Window.

Chip Window Colors and Symbols Color/Symbol	**Definition**
White Border	A white border denotes a selected object.
Black Background	A black background denotes an unused or unplaced module.
Blue	Blue denotes a combinatorial module.
Yellow	Yellow denotes *fixed* logic modules. If the module is selected, the symbol appears yellow. If the module is unselected, the border appears yellow.
Green	Green denotes I/O modules.
Red	Red denotes clock modules.
Magenta	Magenta denotes sequential modules.
	Reserved modules that are not user definable are gray, crossed-out symbols on a black background.
	Clock modules are red. Unused/unplaced modules are red symbols on a black background. Used/placed modules are black symbols on a red background.
	Input/Output modules *are* green. Unused/unplaced modules are green

	symbols on a black background. Used/placed modules are black symbols on a green background.
	Combinatorial modules are blue. Unused/unplaced modules are blue symbols on a black background. Used/placed modules are black symbols on a blue background.
	Sequential modules are magenta. Unused/unplaced modules are magenta symbols on a black background. Used/placed modules are black symbols on a magenta background.
	Buffer modules are blue.
 	RAM modules are green. Unused/unplaced modules are green symbols (RAM) on a black background. Used/placed modules are black on a green background.
 	PLL modules are green. Unused/unplaced modules are green symbols (PLL) on a black background. Used/placed modules are back on a green background.
	I/O FIFO Block Controller modules are green. Unused/unplaced modules are green symbols (IOFCTL) on black backgrounds. A used/placed module is black on a green background.
	I/O FIFO Inbuff modules are pink on a black back ground. Used/placed modules are black on a pink background.
	I/O Inbuff modules are pink on a black background. Used/placed modules are black on a pink background.

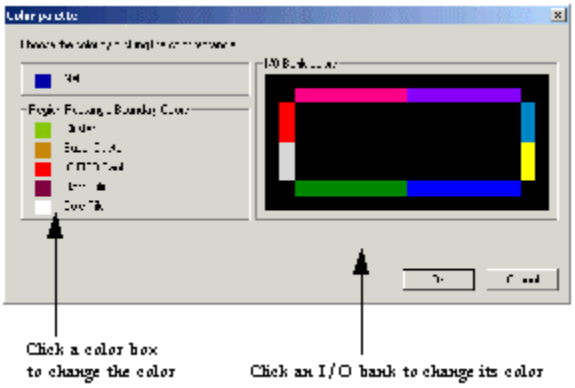


Changing Colors in ChipEditor

Customize the colors used to display I/O banks, clusters, SuperClusters, and nets in the ChipView window by using the Color Manager.

To customize colors in the ChipView window:

1. From the **View** menu, click **Color Manager**.



2. Click the color box in front of the item you wish to customize, or click the I/O bank you wish to change to see the color pallet.

3. Select a new color and click **OK**. The new color appears in the Color Manager dialog box.
4. When you are done customizing your colors using the Color Manager dialog box, click **OK**.

Placed and Unplaced List Boxes

The ChipEditor Placed and Unplaced list boxes display placed or unplaced macros in the design. All placed macros appear in the Placed list box and all unplaced macros appear in the Unplaced list box.

To configure the list boxes:

1. From the **View** menu, click **Configure List Boxes**.
2. In the Configure List Boxes dialog box, select from the following options:

- **Filter Placed and Unplaced Lists**: Entering a macro name in this area will filter for a specific macro or group to be displayed in the Placed or Unplaced list box. You can use the "*" character as a wildcard.
- **Placed List Box Filters**: Use these radio buttons to filter the Placed List Box to display fixed and unfixed macros, only fixed macros, or only unfixed macros.
- **Unplaced List Box Filters**: Use these radio buttons to display all macros or just those that must be manually placed.
- **List Type**: Use the List Type filters to display macro instance names in a flat or hierarchical list in the Placed and Unplaced list boxes. When instance names are displayed hierarchically, collapsed levels are preceded by a plus sign (+) and expanded levels are preceded by a minus sign (-). Clicking the plus sign expands the hierarchy of a macro, while clicking the minus sign collapses the hierarchy. Macros, both fixed and unfixed, are displayed hierarchically by default.

World View Window

Use the World View window to control which portion of the ChipView is displayed in the ChipView window. The blue rectangle (known as the ChipView rectangle) represents the chip. The green rectangle (known as the Viewing rectangle) represents the area displayed in the ChipView window.

To move the displayed area to another part of the chip, click the left mouse button and drag the Viewing rectangle to the area on the ChipView rectangle you would like to display. To specify a new display area, click the right mouse button and drag-out a new Viewing rectangle on the ChipView rectangle.

ChipEditor Status bar

Family, die and package information appears in the right corner of the status bar. In addition, the status bar displays information on commands, pins, placed macros, nets, error messages, and the family, die, and package.

- Hold your mouse over a placed macro in the ChipView window to see the pin number, instance name, net name, macro cell, and fixed or unfixed status in the Status Bar.
- To see nets displayed in the status line, select a macro, zoom in, and click one of the ratsnest lines.
- If you hold your mouse over a toolbar icon or a menu command, a short description of the command function appears in the Status Bar.
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Error messages in the Status Bar provide details about invalid placement attempts. Choose **Help** > **Extended Error Messages** to view more information about the last failed command or placement attempt.

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