SmartPower User's Guide

V6.1

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Printed in the United States of America

Part Number: 502-9136-5/10.04

Release: October 2004

Trademarks

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SmartPower

Welcome to SmartPower

Welcome to SmartPower, Actel's state-of-the-art power analysis tool. SmartPower enables you to identify power consumption problems quickly within a component, then optimize accordingly. SmartPower offers a distinct advantage over lesser power analysis tools by letting you estimate the power of individual components, rather than restricting you to the overall design. SmartPower also generates detailed hierarchical reports of the dynamic power consumption of a design for easy inspection. These reports includes design-level power summary, average switching activity, and ambient and junction temperature readings. You have to simply input the target clock and data frequencies for your design, and let SmartPower perform a detailed and accurate power analysis. SmartPower supports importing files in the VCD (Value-Change Dump) format as specified in the IEEE 1364 standard. It also supports the SAIF (Synopsys' Switching Activity Interchange Format) standard. Support for these formats lets you generate switching activity information in a variety of simulators and then import this information directly into SmartPower.

SmartPower supports ProASIC3/E, ProASIC^{PLUS}, Axcelerator, ProASIC, and RTAX-S families. If you are using any other family, the SmartPower button does not appear on your toolbar. For information on future support for other device families, visit the Actel website at http://www.actel.com.

Invoking SmartPower

Note: When you launch SmartPower, you must first input your target clock and data frequencies before you evaluate your power consumption.

You cannot launch SmartPower if your design is not in a post-layout state in Designer. If you invoke SmartPower before compiling your netlist, Designer guides you through the compile and layout process.

There are three ways to invoke the SmartPower analysis tool:

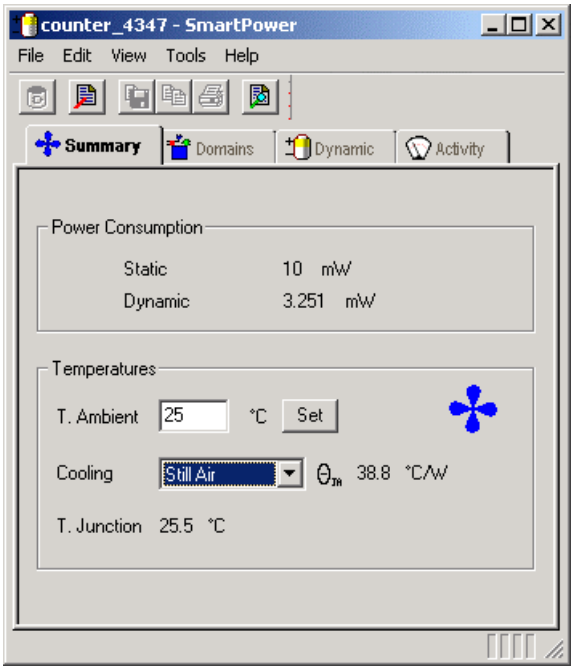
1. Choose **SmartPower** from the **Tools** menu.
2. Click the **SmartPower** icon in the Designer toolbar.
3. Click the **SmartPower** button in Designer design flow.

Note: When you launch SmartPower for the first time, all clocks are assigned a frequency of 10 MHz by default. In addition, SmartPower sets all data frequencies to 1 MHz. To accurately measure the power consumption of a design, you must specify the target clock and data frequencies.

SmartPower Interface

Summary tab

The **Summary** tab is divided into two sections: **Power Consumption** and **Temperatures**.



SmartPower Summary Tab

Power Consumption

Displays the total static and dynamic power of the design. (Accurate only after you have entered your target clock and data frequencies.)

Temperatures

Displays the impact of the power consumption on the junction temperature for a given cooling scenario. You can specify a cooling scenario using the drop-down menu (available scenarios are: Still Air, 300 ft/min, Custom, and Case Cooling; default is Still Air). SmartPower also reports the thermal resistance, θ_{JA}.

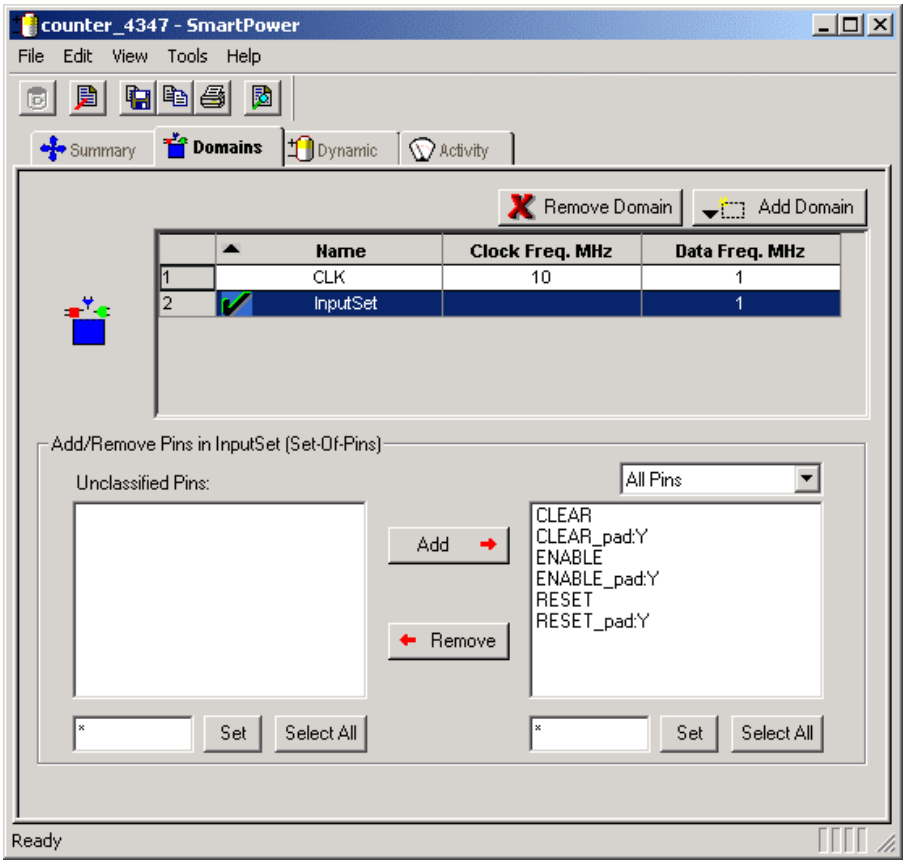
The junction temperature estimation T is dependent on the thermal resistance (θ_{JA}) (which is itself package and cooling-style dependent), and the ambient temperature T_A, and the total dynamic power consumption of your design P. The formula is:

where: $T_J = T_A + P \cdot \theta_{JA}$

$\theta_{JA} = f(\text{Pkg \& Cooling Style})$

Domains tab

The **Domains** tab consists of two windows: the **Domain Management** window and the **Pin Management** window. You can use these windows to add or remove domains. In addition, you can change the clock and/or data frequency of a selected domain.



SmartPower Domains Tab

Domain Management

The **Domain Management** window displays a list of existing domains with their corresponding frequencies.

The **Domain Management** window enables you to create new CLK domains or Set-of-Pins. Also, you can delete or modify existing CLK or Set-Of-Pins domains.

To create a new CLK domain or Set-of-Pins, click **Add Domain** and choose to add a new **Clock Domain** or **Set-Of-Pins**. Input the relevant information (potential clock pin, clock, and data frequency for a clock domain; name and frequency for a pin) and click **Create**.

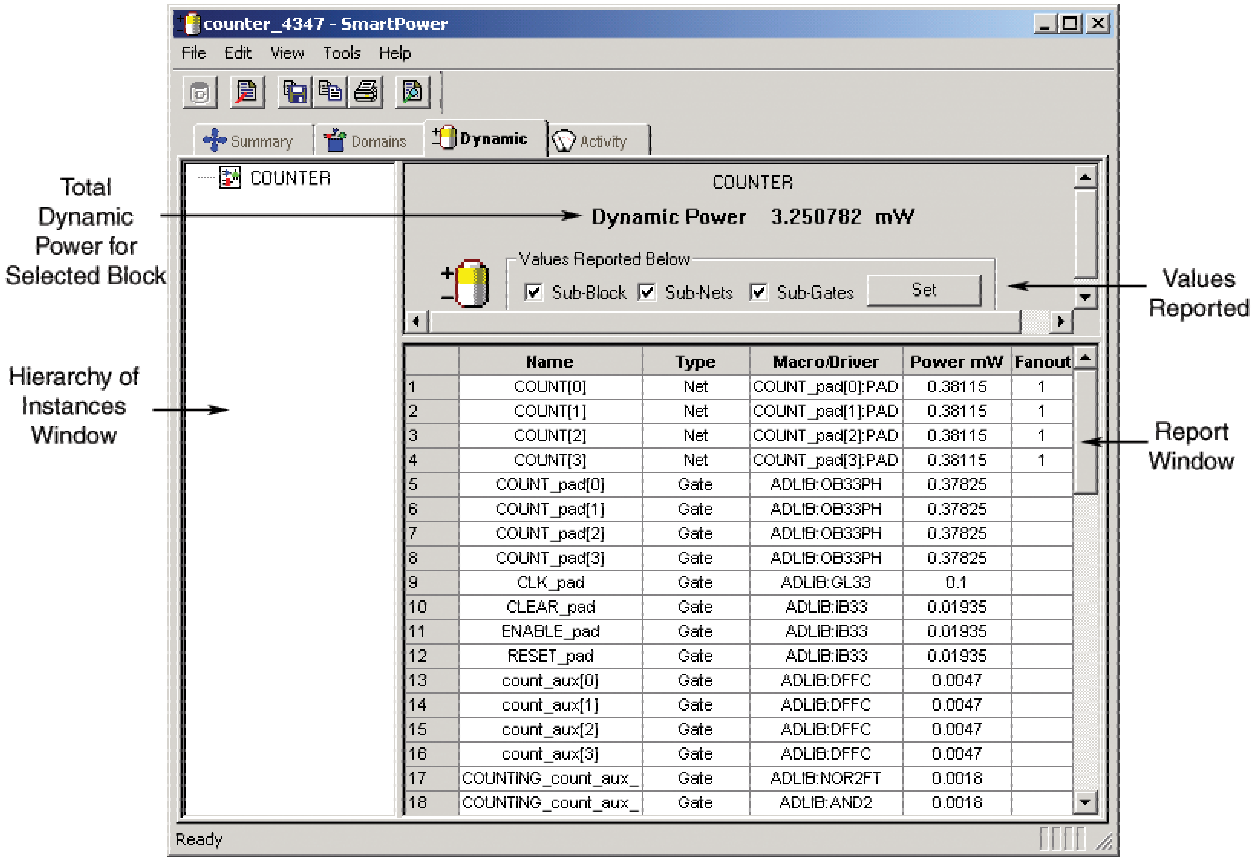
Pin Management

Any pins that do not belong to a domain are listed in the **Unclassified Pins** list box in the Pin Management window. You can select a pin from the **Unclassified Pins** list box and add it to the current domain. You may also select a pin from the current domain and remove it from the domain (this pin will appear in the **Unclassified Pins** list box).

Use the **filter** boxes to narrow your search for a specific pin. The boxes are text filters; * is a wildcard.

Dynamic tab

The **Dynamic** tab enables you to inspect detailed hierarchical reports of the dynamic power consumption. The **Dynamic** tab consists of two windows: the **Hierarchy of Instances** window, and the **report** window.



SmartPower Dynamic Tab

Hierarchy of Instances Window

SmartPower displays the hierarchy of instances in a list in the hierarchy window. Sub-blocks of a block are shown in the tree when you click the plus sign (+) next to the block. Only hierarchical blocks are displayed in this list (no gates or nets).

When you select a block of the hierarchical tree, SmartPower displays its name and its dynamic power consumption in the report window.

Report Window

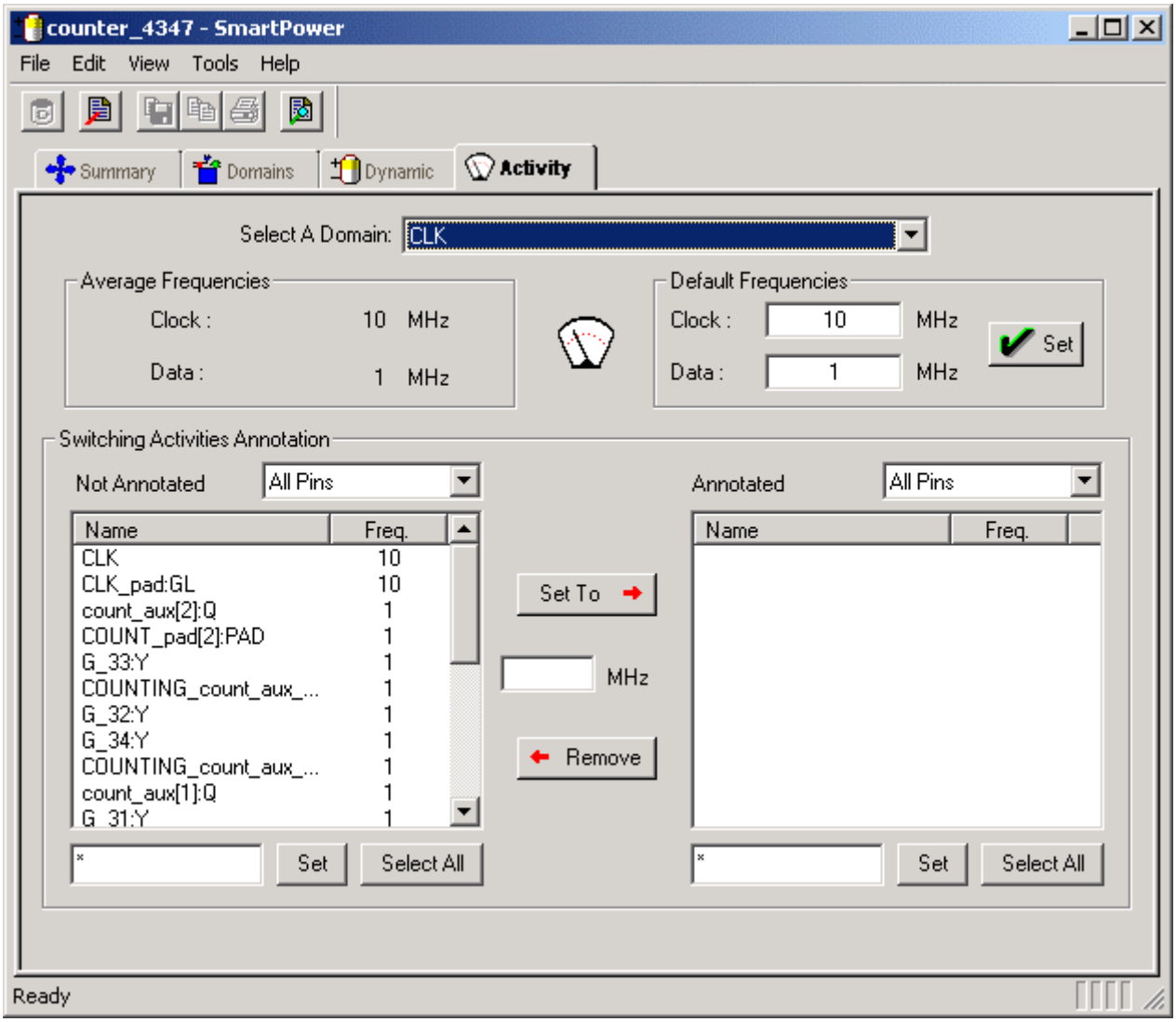
SmartPower displays the list of sub-elements of the selected block in the Report window. By default, this list includes all sub-elements. The dynamic power consumption of each sub-element is displayed with useful information like the fanout and the driver name for a net, or the macro model name for a gate. The tool computes the power of a net on a flattened netlist and reports the result on the user hierarchical netlist on the sub-net connected to the driver.

You may limit the list of sub-elements to a list of sub-blocks, or gates, or nets, or any combination of these three classes of sub-elements. You may also sort the list according to different criteria (double-click a column label to sort the list based on this column, or change the sort-order).

You can export (to a text file) and print the grid that details your design's power consumption. To do so, select the elements of the grid that you wish to export or print, and then from the **File** menu select **Export Grid** or **Print Grid**, respectively.

Activity tab

Use the **Activity** tab to attach switching activity information on interconnects of the design. The Activity tab is divided into the **Select A Domain** drop-down menu, the **Frequency Estimation** area, and the **Switching Activities Annotation** area.



SmartPower Activity Tab

Select a Domain

Specifies the clock domain (or set of pins). Use the drop-down menu to select a different domain.

You can create your own unique set of pins in the **Domains** tab.

Average Frequencies

Includes the average frequency of the clock pins and data pins of the selected clock domain. Use the Select a Domain drop-down menu to choose another clock domain. If you wish, you may select a set of pins rather than a clock domain. If you select a set of pins instead of a clock domain, SmartPower reports only one average frequency (the average frequency of all the pins of the selected set).

Average Frequencies are useful when you import a VCD file or SAIF file. Since these files enable you to specify the frequency of each pin individually, it is often useful to know the average clock pin or data pin frequency for a particular clock domain.

To view the Average Frequencies of a clock domain, click the **Activity** tab, and select a specific domain in the list.

If you did not specify a frequency annotation for any clock pin in this clock domain, the average value is equal to the default clock frequency of the clock domain. If you annotated one or several clock pins, SmartPower takes these specific annotations into account to compute an average value.

If you did not specify a frequency annotation for any data pin in this clock domain, the average value is equal to the default data frequency of the clock domain. If you annotated one or several data pins, SmartPower takes these specific annotations into account to compute an average value.

Default Frequencies

Enables you to specify the global clock frequency and data frequency for the given clock domain (or set of pins). For designs with multiple clocks, SmartPower defaults to the first clock in alphabetical order. If you wish, you may select a set of pins rather than a clock domain. In this case, you can modify only one frequency (this frequency is used for all the pins of the selected set).

Switching Activities Annotation Area

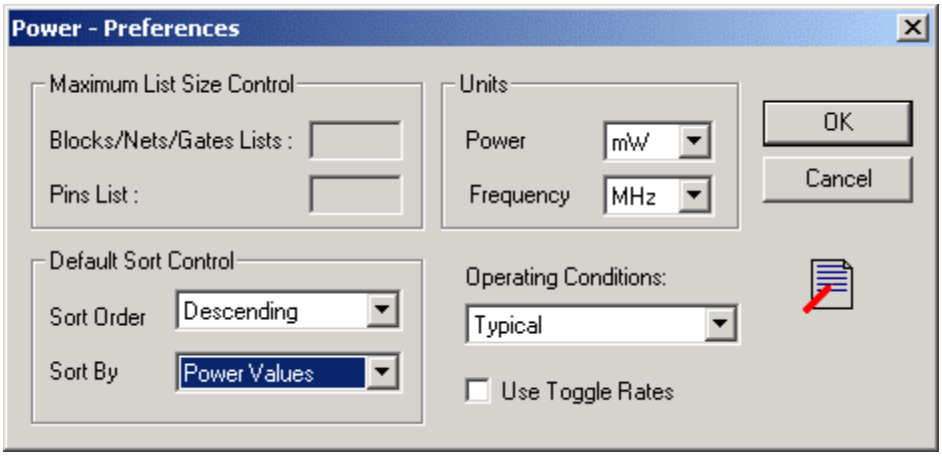
Enables you to specify the switching activities for individual pins in the **Clock Domain**. SmartPower displays the pins that have not been annotated in the **Not Annotated** list box.

Select a pin and specify a different frequency for this pin using the text-box and the **Set To** button. When you select a pin and specify a frequency, SmartPower removes the pin from the **Not Annotated** list-box and adds it to the **Annotated** list-box. Hold down the CTRL key and click with the mouse to select multiple pins.

Use the **Select All** button to select all the pins in a list-box. Filter boxes are provided below the list boxes to limit the size of each list of pins. Enter text in these filter boxes and click **Set** to apply this text as a filter (the ***** character is a wildcard). It is also possible to limit the type of each list of pins using a drop-down menu that enables you select **All-Pins**, **Data-Pins**, or **Clock-Pins**.

SmartPower Preferences

Enables you to set options that affect the graphical and textual reports. To open the SmartPower **Preferences** dialog b ox, from the **File** menu choose **Preferences** or click **Options** in the **Power Report** dialog box.

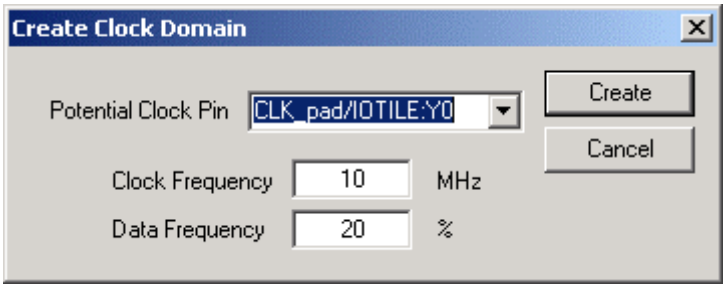


SmartPower Preferences Dialog Box

There are four sections: **Maximum List Size Control**, **Default Sort Control**, **Units**, and **Operating Conditions**.

- **Maximum List Size Control:** Enables you to limit the size of all lists displayed in the SmartPower tab screens (option unavailable at this time).
- **Default Sort Control:** Modifies the default sort for all the lists in SmartPower (available sort keys are Alphabetical or Power values, in either ascending or descending order).
- **Units:** Sets unit preferences for power and frequency.
- **Operating Conditions:** Displays operating conditions; Typical is the only option available at this time.
- **Use Toggle Rates:** When toggle rates are active (**Toggle Rates** box is checked), the data frequency of all the clock domains are defined as a function of the percentage of the clock frequency. This updates the data frequency automatically when you update the clock frequency. Toggle Rates enable you to specify the data frequency as a percentage of clock frequency, but you can no longer specify the actual data frequency, only a percentage value. To see the actual data frequency again, clear the **Use Toggle Rates** option in the **Preferences** window.

Set the data frequency percentage when you create a new clock domain with Toggle Rates active. Also, when toggle rates are active you can set the data frequency percentage in the Domain and Activity tabs.



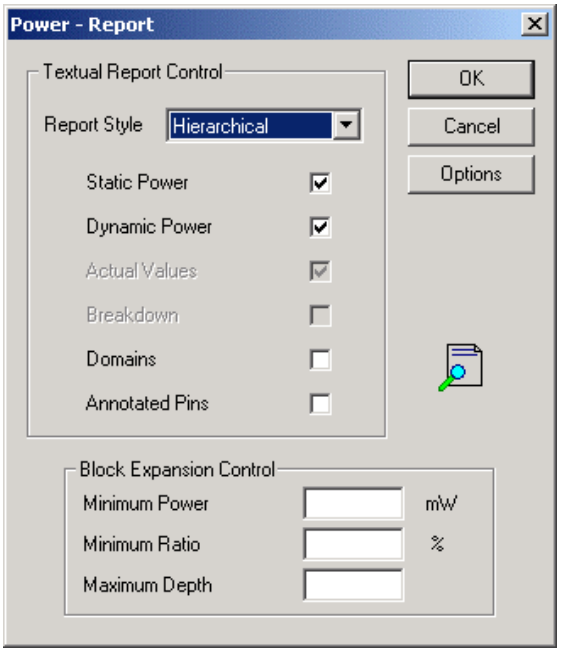
Create Clock Domain - Toggle Rates Enabled

Power Reports

The power report enables you to quickly determine if any power consumption problems exist in your design. The power report lists the following information:

- Global device information and SmartPower Preferences selection information
- Dynamic power summary
- Design-level static power summary
- Hierarchical detailed power report (including gates, blocks, and nets), with a block-by-block, gate-by-gate, and net-by-net power summary

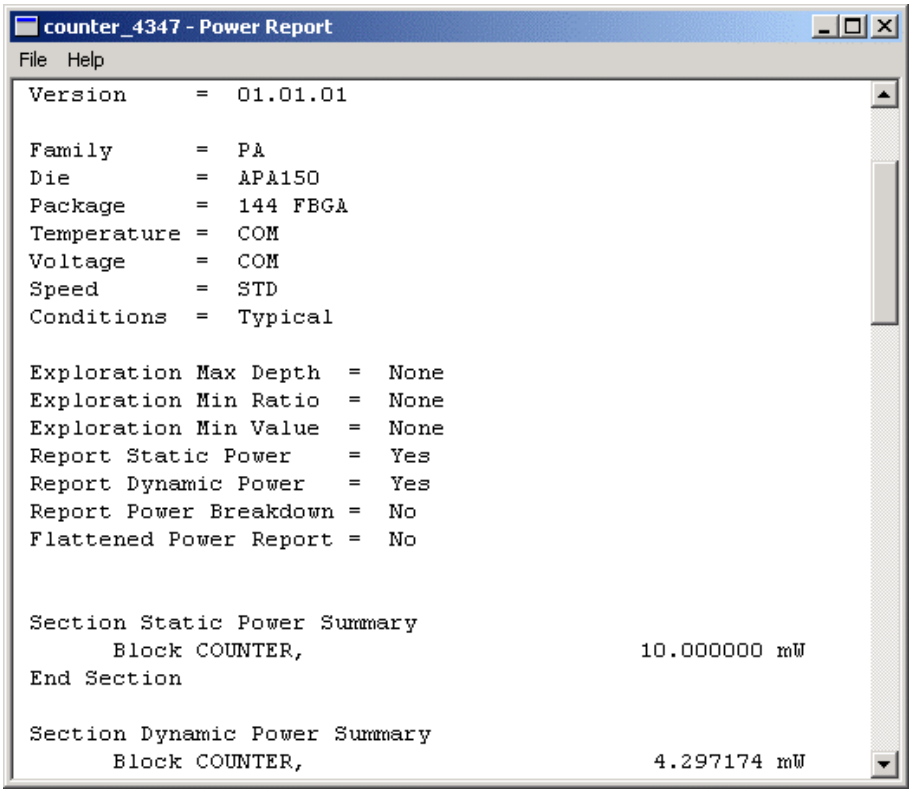
Click the **Report** button to open the **Report** dialog box. Specify which results you want to display (static or dynamic power).



SmartPower Report Dialog Box

The SmartPower report returns a complete list of all the blocks, gates, and nets and the related power consumption in the device (it returns the same information displayed in the Dynamic tab, but it is more printer friendly).

Set the options in the **Textual Report Control** to customize your power report. Select the check boxes to include information on Static Power, Dynamic Power, Domains, and Annotated Pins (actual values are included in all power reports; Breakdown information is not available at this time).



SmartPower Report

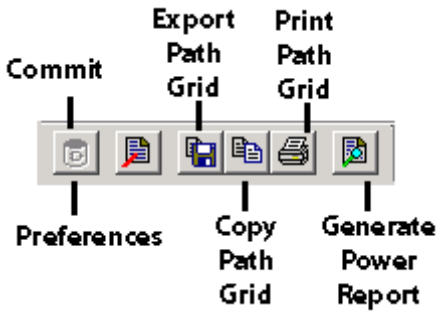
The report fully expands all the information included in the **Dynamic** tab by default; use the **Block Expansion Control** to expand only the blocks you are interested in.

The **Block Expansion Control** options filter the values returned in the report. Block Expansion does not control which values are included (the Textual Report Control options determine content), rather it specifies which blocks are detailed or expanded.

You may specify which blocks are expanded using a Minimum Power value, a Minimum Ratio (with regards to the total power of the design), and a Maximum (hierarchical) Depth; a value filtered by Block Expansion Control is not included in displayed lists, but it is still included in the upper hierarchical analysis of the design. In other words, SmartPower still includes filtered values in the power analysis.

SmartPower toolbar / menu commands

The SmartPower toolbar contains commands for performing common SmartPower operations on your designs. Roll the mouse pointer over the toolbar button to view a description of the button. Click the button to access the command.



SmartPower Toolbar

The PC and workstation versions of SmartPower have the same menus. However, some dialog boxes may look slightly different on the two platforms due to the different window environments. The functionality is the same on both platforms, though the locations of the fields and buttons on the dialog boxes may vary. The names of some fields may also vary between the PC and workstation versions.

File Menu

Commit: Commits power information to Designer. You must commit your changes if you wish to save your settings in SmartPower. If you commit your changes, the information is stored in the .adb file, and your settings are restored the next time you open your design in SmartPower.

Export Grid (enabled in Dynamic tab): Exports the selected area of the **Report** window to a text (.txt) file.

Print Grid (enabled in Dynamic tab): Prints the selected area of the **Report** window.

Preferences: Invokes the **Preferences** dialog box, where you can set analysis and display preferences

Close: Closes SmartPower

Edit Menu

Add Domain (enabled in the Domains tab): Adds a clock domain or set of pins.

Remove Domain (enabled in the Domains tab): Removes a domain.

Copy Grid: Copies the selected cells of the dynamic grid onto the clipboard

Tools Menu

Report Power: Generates power report

Importing a VCD file in Designer

The Value Change Dump (VCD) file is a simulation file. The format of this file is specified in the IEEE 1364 standard.

You can generate a VCD file with a VHDL simulator using the following commands:

```
vcd file example.vcd
vcd add -r *
run 1 us
```

This example creates a VCD file example.vcd, adds all signals recursively, and then runs the simulation for one micro second.

Note: SmartPower has been validated with VCD files generated by Model*Sim*. However, you may use any Verilog/VHDL simulator that offers a VCD dump feature.

Refer to the user manual of your simulation tool for more information on how to generate a VCD file.

To import a VCD file:

1. From the **File** menu in **Designer**, select **Import Auxiliary Files**. Click **Add** to browse to your VCD file and select it. When you have selected a VCD file, click **OK** to continue.

   If you have not yet completed the layout of the design, the design software guides you through place-and-route so that you can import the VCD file. In order to successfully annotate your VCD values to the design, Designer must complete place-and-route even if you generated your VCD file using timing simulation (post-layout).

   You may wish to import multiple VCD files. If these files conflict (attempt to set a different frequency for the same net of your design, for example), the latest imported value takes precedence.

2. Specify your VCD import options. Use the VCD **Import Options** window to specify the instance name of your design in the simulation testbench (the instance name is the instance name of your design instantiated in the simulation testbench). For example, the instance name of the design “top_comp” in the following verilog test-bench is “inst”.

   ```
   module test;
   reg [3:0] DataA, DataB;
   wire AGEB;
   top_comp inst(DataA, DataB, AGEB);
   initial
   begin
   ……
   end;
   endmodule;
   ```

   It also possible to identify the instance name of your design in the VCD file. You have to look for a line starting with the keyword $scope. For example, the instance name of the design “top_comp” in the following VCD file is “inst”.

   ```
   $date
   Oct 18, 2001  16:02:16
   $end
   $version
   VERILOG-XL 3.30.p001
   $end
   $timescale
   100ps
   $end
   $scope module inst $end
   ……
   ```

   Click **OK** to continue.

3. Check the **Log** window for notification that you successfully imported the VCD file ("The Import command succeeded..."). Even if the Import command succeeds, Actel recommends that you use SmartPower to verify which of the pins have been affected after you import the file.

4. Verify results of the imported file in the **Activity** tab screen in SmartPower. To view the results of your imported VCD file, launch SmartPower and navigate to the **Activity** tab screen to view pins with annotated switching activities. If your file was imported successfully, you will see a long list of pins with annotated switching activity and specific individual frequencies.

It may be that some pins of your design are not annotated by a VCD import command. This happens if you simulate a pre-synthesis netlist; it is normal because not all logic elements are in the pre-synthesis netlist. Thus, for accurate power estimation, it is better to run post-layout simulation with a back-annotated netlist.

Importing a SAIF file in Designer

Use the following instructions to import a SAIF file.

To import a SAIF file:

1. From the **File** menu in **Designer**, select **Import Auxiliary Files**. Click **Add** to browse to your SAIF file and select it. When you have selected a SAIF file, click **OK** to continue.

   If you have not yet completed the layout of the design, the design software guides you through place-and-route so that you can import the SAIF file. In order to successfully annotate your SAIF values to the design, Designer must complete place-and-route even if you generated your SAIF file using timing simulation (post-layout).

   You may wish to import multiple SAIF files. If these files conflict (attempt to set a different frequency for the same net of your design, for example), the latest imported value takes precedence.

2. Specify your SAIF import options. Use the SAIF **Import Options** window to specify the instance name of your design in the simulation testbench (the instance name is the instance name of your design instantiated in the simulation testbench). **You must include the hierarchy with the instance name.**

   The example below shows how to identify the instance name of your design in the SAIF file. For example, the instance name of the design in the following SAIF file is "TEST_BENCH/UUT".

```
(SAIFILE
(SAIFVERSION "1.1")
(DESIGN 2ff)
(DATE "Fri May 10 14:48:46 2002")
.....
(TIMESCALE 1ns)
(DURATION 50000)
(INSTANCE TEST_BENCH/UUT (PORT (OUT_PORT (TC 26) (IG 0) (T1 25994)
(T0 22000) (TX 2006))))
(INSTANCE TEST_BENCH/UUT/\outpad/U0/U1\ (PORT (Y (TC 26) (IG 0)
(T1 25995) (T0 22000) (TX 2005))))
(INSTANCE TEST_BENCH/UUT/\ff1/U0\ (PORT (Q (TC 27) (IG 0) (T1 26000)
(T0 22997) (TX 1003))))
(INSTANCE TEST_BENCH/UUT/\clkpad/U0/U0\ (PORT (Y (TC 99) (IG 0)
(T1 25000) (T0 24999) (TX 1))))
```

.....

Click **OK** to continue.

3. Check the **Log** window for notification that you successfully imported the SAIF file ("The Import command succeeded..."). Even if the Import command succeeds, Actel recommends that you use SmartPower to verify which of the pins have been affected after you import the file.

4. Verify results of the imported file in the **Activity** tab screen in SmartPower. To view the results of your imported SAIF file, launch SmartPower and navigate to the **Activity** tab screen to view pins with annotated switching activities. If your file was imported successfully, you will see a list of pins with annotated switching activity and specific individual frequencies.

It may be that some pins of your design are not annotated by a SAIF import command. This sometimes happens if you simulate a pre-synthesis netlist. It is normal; not all logic elements are in the pre-synthesis netlist. Thus it is better to do a post-layout simulation with a back-annotated netlist for the most accurate power estimation.

Calculating Power

Steps to calculate power

Use the steps below to calculate your power consumption. The steps are identified by the tabs you should view (in the order you should view them) so that you may analyze your power accurately.

1. Domains tab - Define clock domains and specify a clock frequency and a data frequency for each clock domain.
2. Activity tab - Specify individual pin frequencies, this step is optional, but gives you a pin-by-pin control of the frequency.
3. Summary tab - View global power at the design level and view its impact on junction temperature.
4. Dynamic tab - View detailed hierarchical analysis of your power consumption. This step is also optional. But if your power consumption exceeds your budget, this step will help you to understand where there is room for improvement.

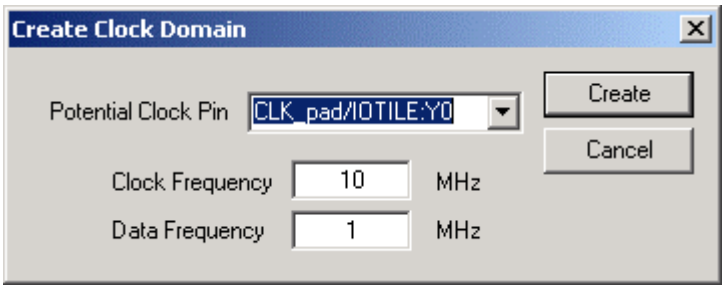
Defining Clock Domains

Define clock domains and Set-of-Pins

When you run SmartPower, it researches your existing clock domains and partitions your design automatically. You may wish to review the list of clock domains in the Domains tab to ensure that all the clocks of your design are included in the list. Add or remove clocks as necessary.

To add a new clock domain:

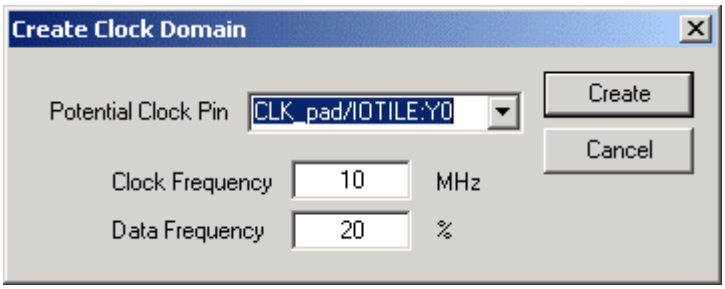
1. Click the **Domains** tab, and click the **Add Domain** button. Select **Clock Domain** from the drop-down menu. This opens the **Create Clock Domain** dialog box.



Create Clock Domain Dialog Box - Toggle Rates Disabled

2. To create a new clock, select a **Potential Clock Pin**, specify a clock and data frequency, and click **Create**. The new clock domain appears in the **Domains** window. If you select an existing clock pin from the drop-down menu, the lists of clock pins and data pins of this new clock domain are computed automatically based on the netlist topology.

   Note: Select Use Toggle Rates in the SmartPower Preferences to define your data frequency as a percentage of your clock frequency. If your data frequency is 20% of your clock frequency, type "20" in the Data Frequency text box.



Create Clock Domain Dialog Box - Toggle Rates Enabled

   You may wish to create an empty clock domain and fill the lists of clock-pins and data pins manually. If so, do not select a clock pin, just type a new name for your clock domain.

Beyond the verification of the list of clock domains, you may also wish to verify that the lists of clock pins and data pins computed for each clock domain are correct.

To verify the lists of clock pins and data pins of a clock domain:

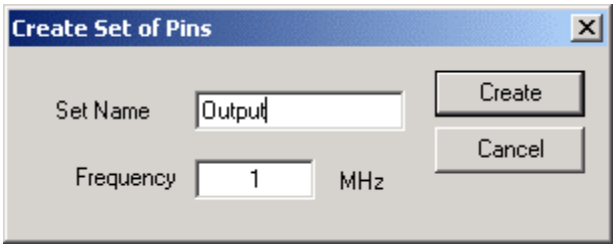
1. To select a Clock Domain, click the **Domains** tab, and select a specific **Domain** in the list.
2. **Display the list of clock pins or data pins of this Domain.** A drop-down menu in the **Domain** tab enables you to select clock pins or data pins. SmartPower displays the list of pins corresponding to your selection below the drop-down menu. You can add or remove clock pins and data pins as necessary.
3. **Remove a pin from a clock domain.** Highlight the selected pin and click the **Remove** button. The pin is removed from the clock domain, and is made available in the list of pins that you can add in another clock domain.
4. Highlight the selected pin in the list of pins that are not yet in a domain and click the Add button to add a pin in a clock domain. This pin is added to the clock domain. It is a clock pin or a data pin, depending on the specification of the drop-down menu when you click the **Add** button.

Note: You cannot add a pin that exists in another domain until you free it from the existing domain. The pin is unavailable until you remove it from that domain.

After you have verified that all the clocks of your designs are correctly identified and constructed, you must specify the correct clock and data frequency for each clock domain.

To add a new set of pins:

1. Open the **Create Clock Domain** dialog box. Click the **Domains** tab, and click the **Add Domain** button. Select **Set of Pins** from the drop-down menu.



Create Set of Pins Dialog Box

2. **Create a Set of Pins.** Name your new Set of Pins, specify a data frequency, and click **Create**. The new Set of Pins appears in the **Domains** window.

Specify clock and data frequencies in SmartPower

To specify a clock and data frequency, select the **Clock/Data** frequency cell and type in a new value.

SmartPower defaults to 10 MHz for each clock frequency, and 1 MHz for the data frequency. Input your target for each clock and data frequency (5% of your clock frequency is a typical guideline for your data frequency - this corresponds to a toggle rate of 10%.)

Not all the pins/gates/nets of your design are associated with a specific clock. For example, the frequency of a design input port is not always correlated to a clock frequency. By extension, all pins that are upstream of the first level of sequential elements are not associated with any clock. SmartPower creates an InputSet by default that it uses to group all the pins that are controlled by design inputs (instead of sequential elements). You may wish to view and verify the InputSet to further evaluate your design.

View and verify the InputSet in SmartPower

To verify the InputSet:

1. Click the **Domains** tab and select the domain named **InputSet** in the list.
2. Verify the list of pins of this Domain. All the input ports of your design (except the clocks) belong in the **InputSet**. Also, all the pins that are between these input ports and the first level of sequential elements belong in the **InputSet**. You can add or remove pins as necessary.
3. Specify an average input frequency. SmartPower uses the same frequency for all pins of the InputSet. The default InputSet frequency is 1 MHz. Type in a new value to change it.

You may wish to split the InputSet into several sets in order to specify different frequencies. A classic example is to create a ResetSet, a reset tree with a very low frequency.

To split the InputSet into several sets:

1. Create a new Set of Pins. In the **Domains** tab, click the **New** button, and select **Set of Pins** from the drop-down menu. In the **Create Set Of Pins** dialog box, type a name and a frequency for the new set and click **Create**. The new set of pins appears in the **Domains** window. You can only create an empty set of pins, but it is possible to add pins in this Domain latter.
2. Remove a group of pins from the **InputSet**. Click the **Domains** tab and select the domain named **InputSet** in the list. Select the pins that you want to remove and click the **Remove** button.
3. Add this group of pins in the new set of pins. Click the **Domains** tab and select the newly created set of pins in the list. Highlight the pins in the list of pins that are not yet in a domain, and click the **Add** button. Repeat these three steps as necessary to create multiple inputs sets.

Specify individual pin frequencies

The Activity tab enables you to specify an average clock and data frequency for each clock domain, and also an average frequency for each set of pins. This gives you an initial estimate of the power consumption of your design. However, if this estimate is not accurate enough, you may refine it with a pin-by-pin annotation of the frequency.

To specify a frequency annotation for an individual pin:

1. Locate the pin in the Activity tab. You may need to select different clock domains from the drop-down menu on the **Activity** tab, then search in the **Not-Annotated Pins** list to find the specific pin. You can use filters to facilitate this search.
2. Select the pin in the list of **Not Annotated** pins, enter a new frequency value, and click the **Set To** button. This specifies a new frequency for the selected pin. The pin with this new frequency appears in the list of **Annotated** pins. Repeat these two steps as necessary to annotate the frequency of several pins.

Note: This annotation procedure enables you to set the frequency of an individual pin, but this does not mean that the pin is removed from its clock domain. A frequency annotation just overrides the domain level frequency.

You may wish to change or remove a frequency annotation of an individual pin. This may be useful when you import a VCD (value change-dump) file or a SAIF (Switching Activity Interchange Format) file.

To change the frequency annotation of an individual pin:

1. Locate the pin in the **Activity** tab**.** You may need to select different clock domains from the drop-down menu on the **Activity** tab, and then search in the **Annotated Pins** list to find the specific pin. You can use filters to facilitate the search.
2. Select the pin in the list of **Annotated** pins, enter a new frequency value, and click the **Set To** button. This specifies a new frequency for this pin. The pin appears in the list of annotated pins with this new frequency. Repeat these two steps as necessary to change the frequency annotation of several pins.

To remove the frequency annotation of an individual pin:

1. Locate the pin in the **Activity** tab. You may need to select different clock domains from the drop-down menu on the **Activity** tab, and then search in the **Annotated Pins** list to find the specific pin. You can use filters to facilitate the search.
2. Select the pin in the list of **Annotated** pins and click the **Remove** button. This removes the specified frequency from the Annotated pin. The pin appears in the list of **Not Annotated** pins. Repeat these two steps as necessary to remove the frequency annotation of several pins.

View results (design level)

Click the Summary tab to view global power consumption at the design level. The **Summary** tab shows your designs' estimated **Power Consumption** and **Temperature** information.

The power estimation reported in the **Summary** tab is the total static and dynamic power consumption of your design. For a more detailed view of this power consumption, click the Dynamic tab.

To estimate the junction temperature:

1. Verify your package. You cannot change your package directly in SmartPower, because it may obsolete your place-and-route information (and thus it may severely impact the total power consumption). If you wish to choose another package, you have to do it in **Designer > Tools > Device Selection**.
2. Click the **Summary** tab, and select a **Cooling** style in the list. Thermal resistance changes automatically when you update the cooling style.
3. Specify an ambient temperature. Enter an **ambient temperature** (default value is 25ºC), and click the **Set** button.

Note: The junction temperature value changes according to the package, cooling style, and ambient temperature values you choose.

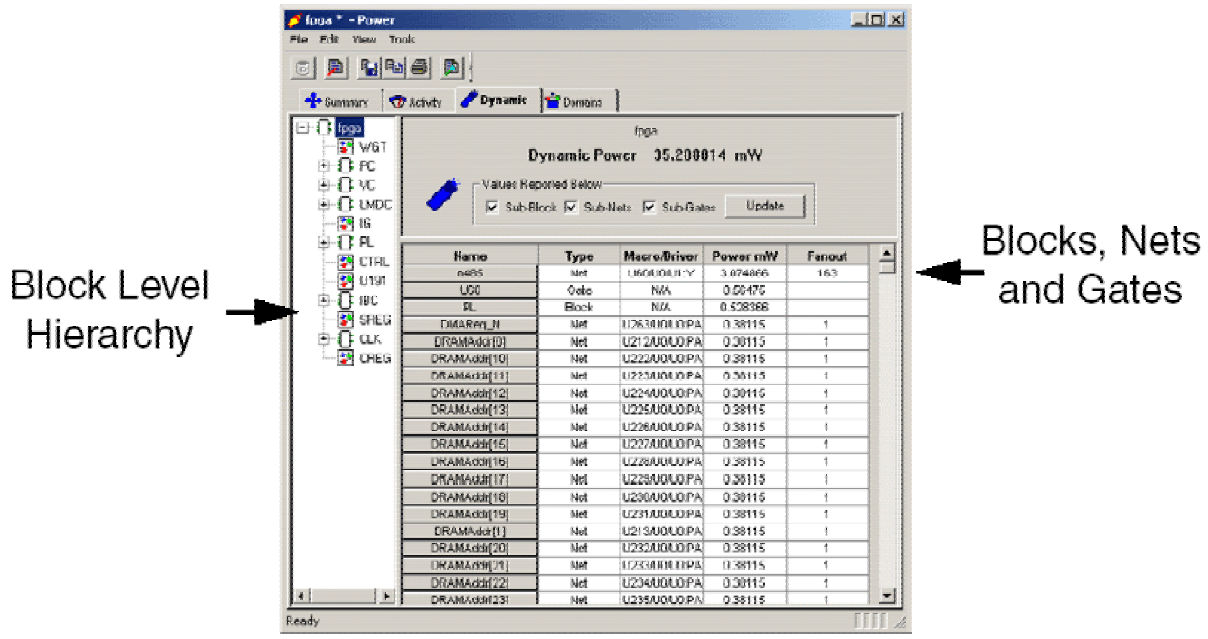
Analyze results

The Dynamic tab displays the estimated power consumption of individual blocks, gates, and nets and enables you to make a hierarchical analysis of your power consumption. The **Dynamic** tab may also help you to improve your power consumption by identifying the blocks, gates, and nets consuming a significant amount of power.

You can export (to a text file) and print the grid that lists your design's power consumption. To do so, select the elements of the grid that you wish to export or print, and then from the **File** menu select **Export Grid** or **Print Grid**, respectively.

To identify the blocks, gates, or nets that are consuming the most power:

1. **Use the Dynamic tab to expand the design hierarchy.** The **Dynamic** tab enables you to expand your design hierarchy and view a complete list of the blocks in your design. Click the + next to your design to view the hierarchy. Click the + next to a sub-block to view its sub-elements. Consider the figure below, which shows an example of a clock pin with high fanout.



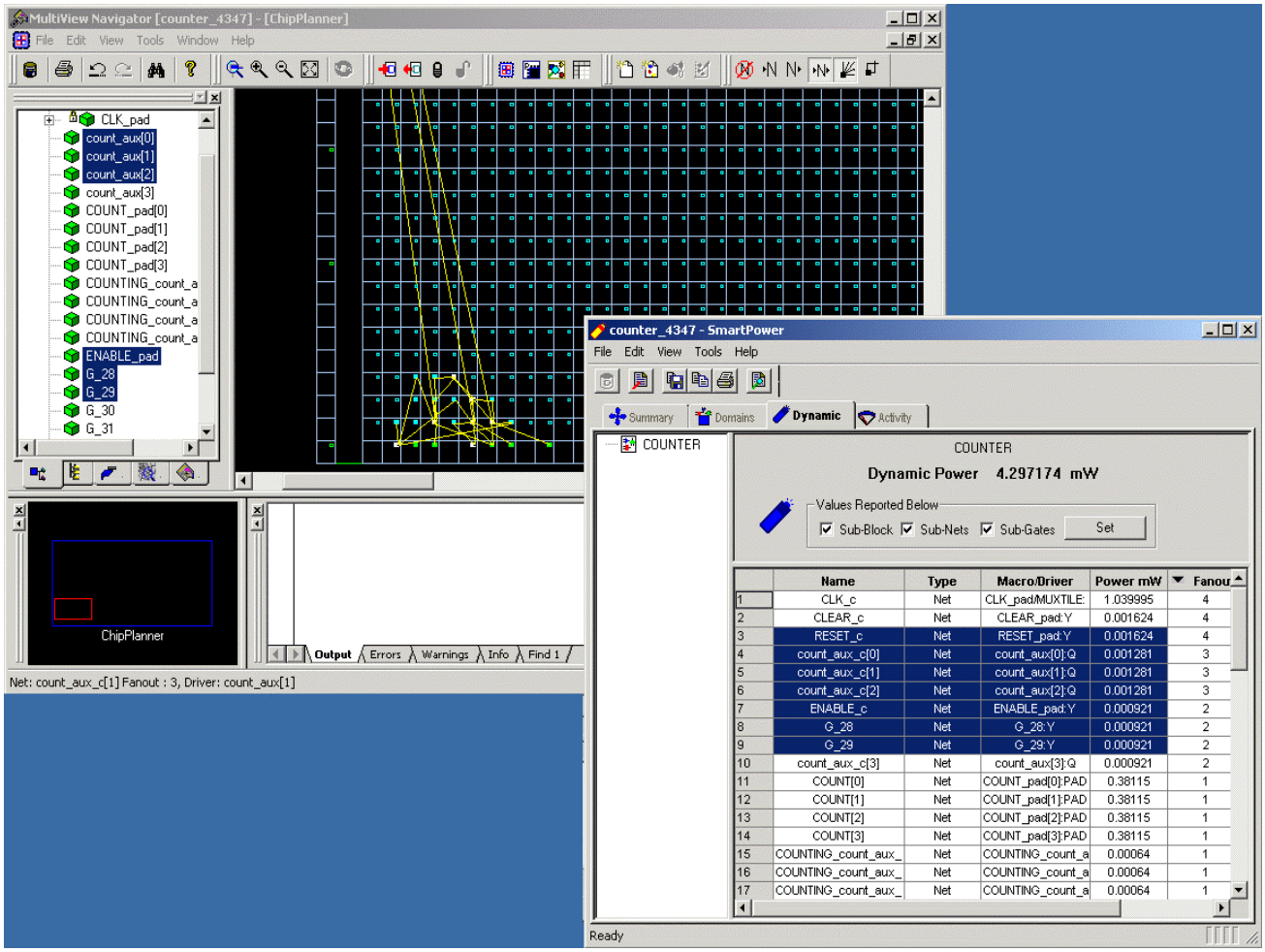
2. **Click to select a block.** By default SmartPower selects the design-level block, but you can always select another block in the hierarchical tree. The **Report** window displays the list of sub-elements of the selected block. By default, this list includes all sub-elements. SmartPower displays the dynamic power consumption of each sub-element with useful information like the fanout and the driver name for a net, or the macro model name for a gate.
3. **Sort and filter the sub-elements to find the block, gate, or net that is using the most power.** Double-click a column heading to sort by that column (or to change the sort order). By default, SmartPower sorts the sub-elements according to their power consumption. The top of the list of sub-elements gives you the main sources of dynamic power consumption at the hierarchical level. Select a check box to limit the list of sub-elements to a list of gates, nets, or blocks.

Cross probing with SmartPower

SmartPower supports cross probing with the other Designer tools. You must calculate your design's power consumption before you can cross probe effectively. See the Calculating Power section for more information.

To cross probe with the SmartPower tool:

1. View the detailed results of your power analysis in the **Dynamic** tab of the SmartPower tool.
2. Open the **ChipPlanner** or the **PinEditor** tool in Designer.
3. Click a block, net, or gate in the **Dynamic** tab to highlight the corresponding component in the **ChipPlanner** or **PinEditor** tool.
4. Click the **Macro/Driver** or **Name** column to cross probe gates.
5. Click an object in the **Name** column to select individual nets; click an object in the **Macro/Driver** column to select the object connected to the net.



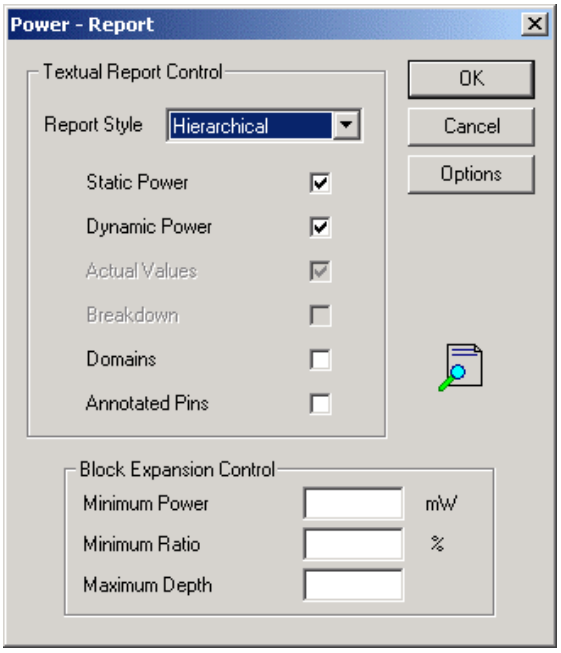
Cross Probing with SmartPower

Power Reports

The power report enables you to quickly determine if any power consumption problems exist in your design. The power report lists the following information:

- Global device information and SmartPower Preferences selection information
- Dynamic power summary
- Design-level static power summary
- Hierarchical detailed power report (including gates, blocks, and nets), with a block-by-block, gate-by-gate, and net-by-net power summary

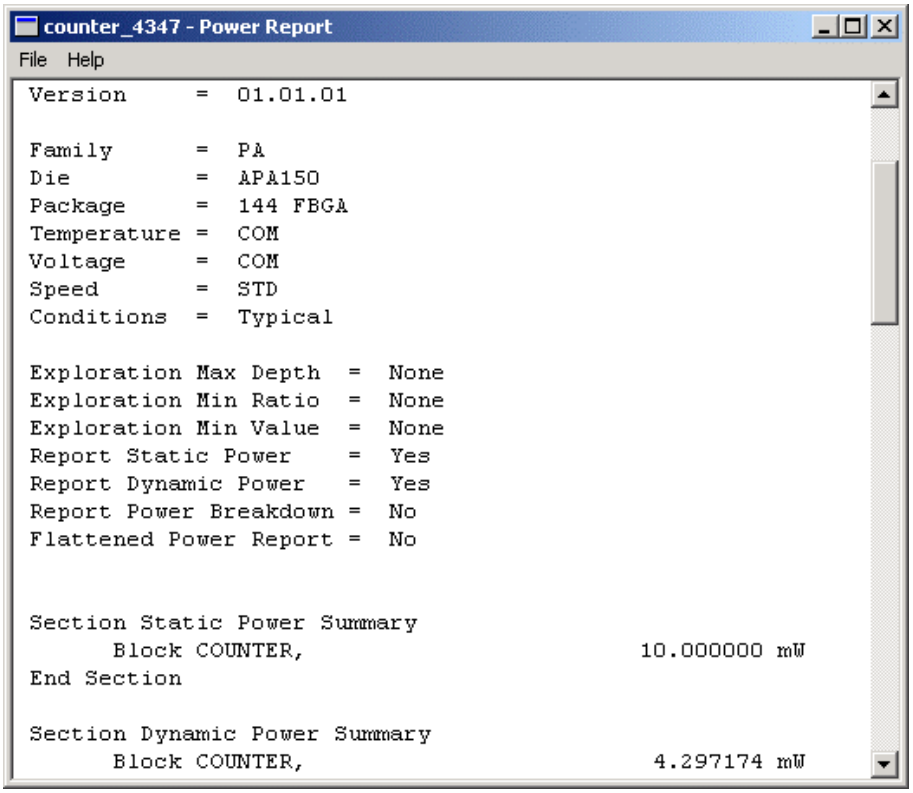
Click the **Report** button to open the **Report** dialog box. Specify which results you want to display (static or dynamic power).



SmartPower Report Dialog Box

The SmartPower report returns a complete list of all the blocks, gates, and nets and the related power consumption in the device (it returns the same information displayed in the Dynamic tab, but it is more printer friendly).

Set the options in the **Textual Report Control** to customize your power report. Select the check boxes to include information on Static Power, Dynamic Power, Domains, and Annotated Pins (actual values are included in all power reports; Breakdown information is not available at this time).



SmartPower Report

The report fully expands all the information included in the **Dynamic** tab by default; use the **Block Expansion Control** to expand only the blocks you are interested in.

The **Block Expansion Control** options filter the values returned in the report. Block Expansion does not control which values are included (the Textual Report Control options determine content), rather it specifies which blocks are detailed or expanded.

You may specify which blocks are expanded using a Minimum Power value, a Minimum Ratio (with regards to the total power of the design), and a Maximum (hierarchical) Depth; a value filtered by Block Expansion Control is not included in displayed lists, but it is still included in the upper hierarchical analysis of the design. In other words, SmartPower still includes filtered values in the power analysis.

Power Calculation Theory

SmartPower equations

SmartPower calculates two power values for your design:

- Static Power: This value is family and die-size dependent and is estimated at the design level. SmartPower provides only the STATIC power consumption of the array.
- Dynamic Power: This value is a summation of the dynamic power consumed by each element of the design (nets, modules, I/Os, RAM, FIFO, PLL, etc.).

Note: The examples below are for general evaluation purposes only. They are not a precise representation of the actual calculations, since each calculation takes into account family-specific information.

Sample Equations:

- For a **net**,
  $$P = C \cdot V^2 \cdot F$$
  where C is the total capacitive loading of the net (extracted from the routing topology), V is the net's voltage swing, and F is the average switching frequency.
- For a **module**, the power is computed using a characterized library (by family and die-size) describing a specific power model for each type of module. For example, the power model of a flip-flop is given by
  $$P = P_{CK} \cdot F_{CK} + P_{DOUT} \cdot F_{DOUT} + P_{Din} \cdot F_{Din}$$
  where F_{CK} is the average clock-input frequency for this flip-flop, F_{DOUT} is its average data-output frequency, and P_{CK}, P_{DOUT}, P_{Din} are three constants estimated by electrical simulation and silicon characterization for this flip-flop module, and F_{Din} is its average data-input frequency.
- For an **I/O**, the formula used for computing the power consumption depends on the I/O technology and the family. For example, for a TTL output, the dynamic power is given by
  $$P = P_{INT} \cdot F + C \cdot V^2 \cdot F$$
  where C is the output load (derived from what you have set in the PinEditor GUI, typically 35 pF for TTL), V is the output's voltage swing (3.3 V for TTL), and P_{INT} represents an internal power contribution dissipated in the pad, and F is the average switching frequency of the I/O.
- For a **complex block**, like a RAM, a FIFO, or a PLL, SmartPower uses a high-level power model that integrates design parameters.

SmartPower automatically computes all the constant parameters of these equations. However, the frequencies depend on the target frequencies of your design. Since it is impractical to enter each frequency manually, SmartPower has several flows that help you to estimate the frequencies and calculate the power consumption.

SmartPower Tcl Commands

SmartPower supports the following Tcl scripting commands:

- smartpower_add_pin_in_domain
- smartpower_commit
- smartpower_create_domain
- smartpower_remove_domain
- smartpower_remove_pin_frequency
- smartpower_remove_pin_of_domain
- smartpower_restore
- smartpower_set_domain_frequency
- smartpower_set_pin_frequency

Refer to Designer online help or *Designer User's Guide* for details.

Contacting Actel

Actel Headquarters

Actel Corporation is a supplier of innovative programmable logic solutions, including field-programmable gate arrays (FPGAs) based on Antifuse and Flash technologies, high-performance intellectual property (IP) cores, software development tools, and design services targeted for the high-speed communications, application-specific integrated circuit (ASIC) replacement, and radiation-tolerant markets.

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UNIX help known issues

Related Topics Links Appear Broken

UNIX (Linux and SOL) do not support links in Related Topics buttons that point to different directories. This has to do with the way the help is built for UNIX systems.

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502-9136-5/10.04