XC4000E IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000E devices unless otherwise noted.

	Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Propagation Delays (TTL Inputs)											
Pad to I1, I2											
Pad to I1, I2 via transparent	T_{PID}	All devices		3.0		2.5		2.0		1.4	ns
latch, no delay											
with delay	T_{PLI}	All devices		4.8		3.6		3.6		2.8	ns
	T_{PDLI}	XC4003E		10.4		9.3		6.9		6.4	ns
		XC4005E		10.8		9.6		7.4		6.5	ns
		XC4006E		10.8		10.2		8.1		6.9	ns
		XC4008E		10.8		10.6		8.2		7.0	ns
		XC4010E		11.0		10.8		8.3		7.3	ns
		XC4013E		11.4		11.2		9.8		8.4	ns
		XC4020E		13.8		12.4		11.5		9.0	ns
		XC4025E		13.8		13.7		12.4		–	ns
Propagation Delays (CMOS Inputs)											
Pad to I1, I2	T_{PIDC}	All devices		5.5		4.1		3.7		1.9	ns
Pad to I1, I2 via transparent											
latch, no delay	T_{PLIC}	All devices		8.8		6.8		6.2		3.3	ns
with delay	T_{PDLIC}	XC4003E		16.5		12.4		11.0		6.9	ns
		XC4005E		16.5		13.2		11.9		7.0	ns
		XC4006E		16.8		13.4		12.1		7.4	ns
		XC4008E		17.3		13.8		12.4		7.4	ns
		XC4010E		17.5		14.0		12.6		7.8	ns
		XC4013E		18.0		14.4		13.0		9.0	ns
		XC4020E		20.8		15.6		14.0		9.5	ns
		XC4025E		20.8		15.6		14.0		–	ns
Propagation Delays											
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		5.6		2.8		2.8		2.7	ns
Clock (IK) to I1, I2											
(latch enable, active Low)	T_{IKLI}	All devices		6.2		4.0		3.9		3.2	ns
Hold Times (Note 1)											
Pad to Clock (IK), no delay	T_{IKPI}	All devices	0		0		0		0		ns
with delay	T_{IKPID}	All devices	0		0		0		0		ns
Clock Enable (EC) to Clock (IK),											
no delay	T_{IKEC}	All devices	1.5		1.5		0.9		0		ns
with delay	T_{IKECD}	All devices	0		0		0		0		ns

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.