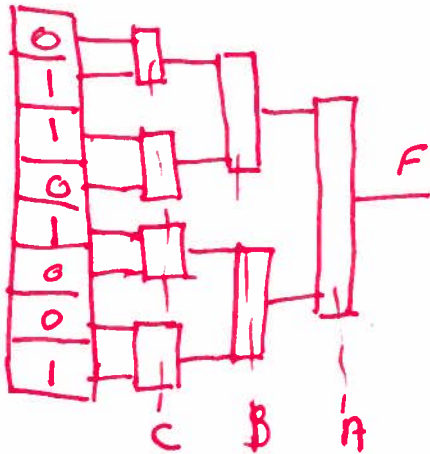
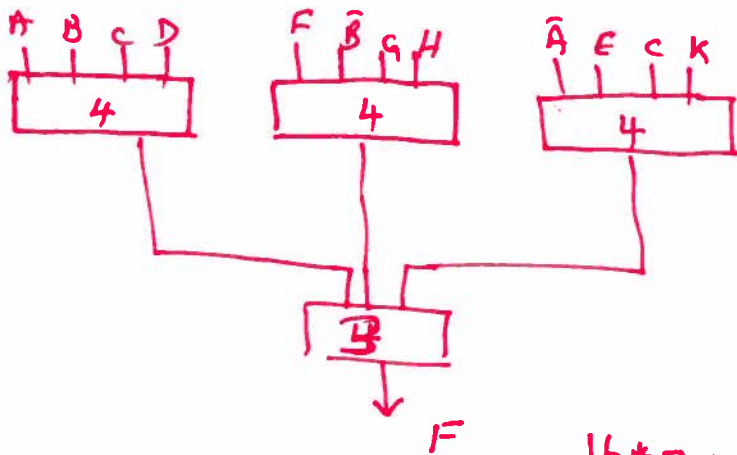


Question 1

a) $F(A, B, C) = \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C = \sum m(1, 2, 4, 7)$



b)



$16 * 3 + 8 = 56$ bits storage

$3 * 2^4 - 1 + 1 * 2^3$ Muxes

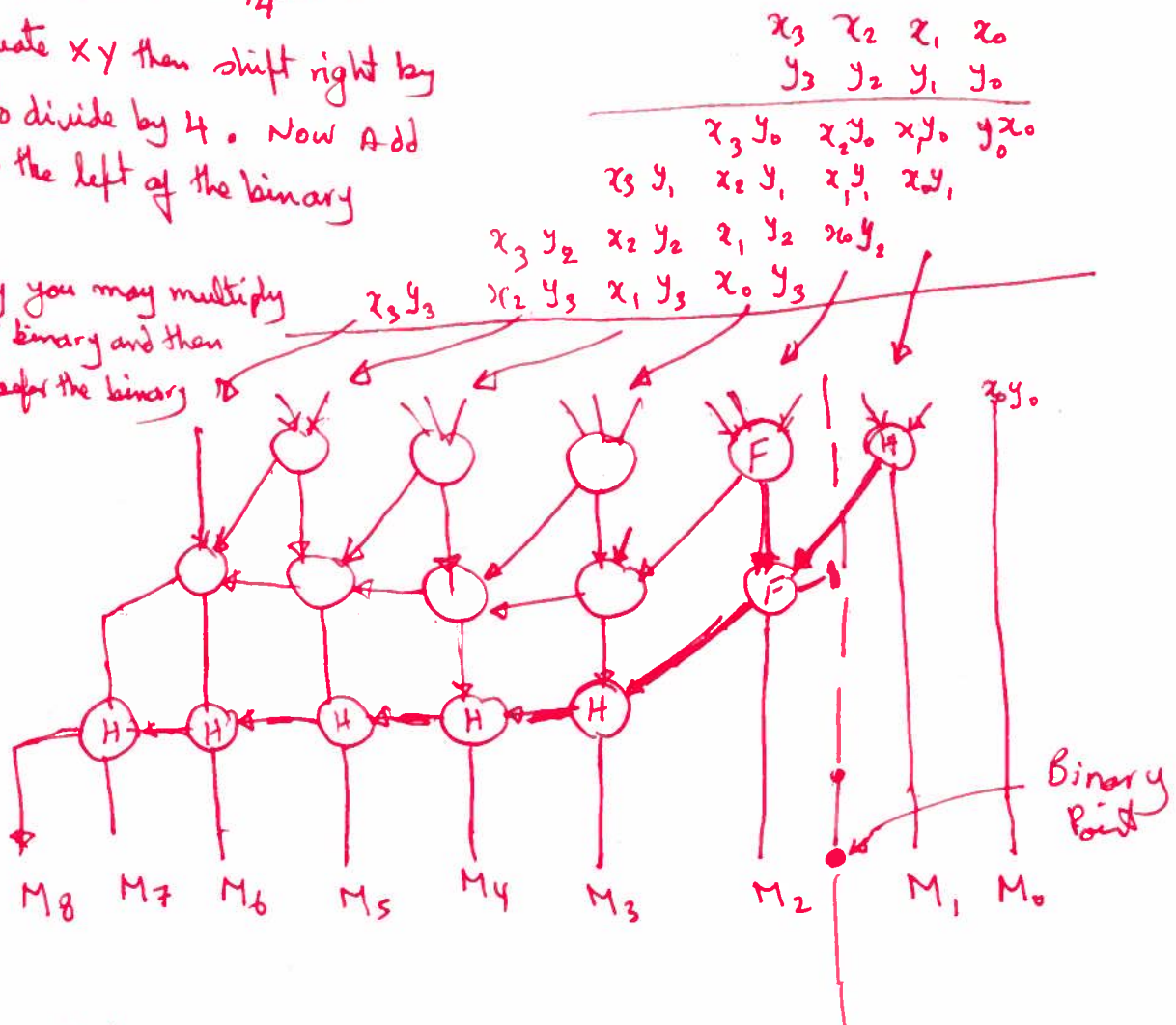
$(4) + (3)$ Mux Delay

COEN 6501 Final Dec 12, 2015

$$Z = 0.25xy + 1 = \frac{1}{4}xy + 1$$

First Evaluate xy then shift right by 2 places to divide by 4. Now Add the '1' to the left of the binary point.

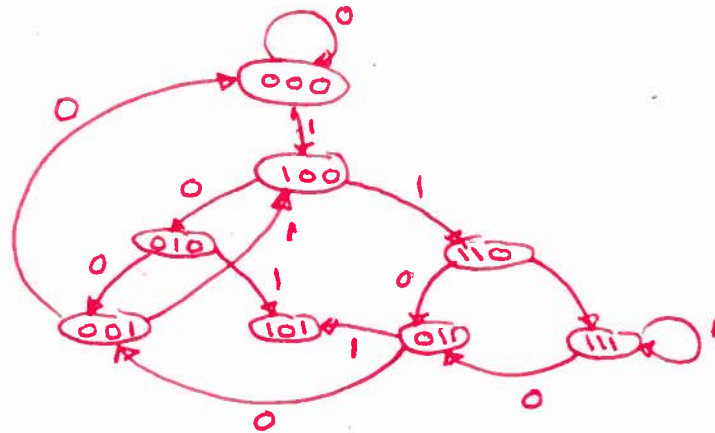
Alternatively you may multiply xy by 0.01 binary and then add the 1 before the binary point



Area 9 Full Adders + 16 AND gate

Delay 2 Full Adder + 5 Half Adder delay + AND gate delay

Question 3



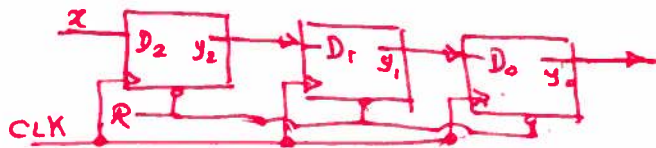
Present state y ₂ y ₁ y ₀	Next state	
	x=0	x=1
0 0 0	0 0 0	1 0 0
0 0 1	0 0 0	1 0 0
0 1 0	0 0 0	1 0 0
0 1 1	0 0 0	1 0 0
1 0 0	0 1 0	1 1 0
1 0 1	0 1 0	1 1 0
1 1 0	0 1 0	1 1 0
1 1 1	0 1 0	1 1 0

From the Transition Table

$$y_2^+ = x = D_2$$

$$y_1^+ = y_2 = D_1$$

$$y_0^+ = y_1 = D_0$$



Question 4

- a) There are 3 paths:
- Path 1 $U_4 \rightarrow U_3 \rightarrow U_5$
 - Path 2 $U_5 \rightarrow U_2 \rightarrow U_4$
 - Path 3 $U_5 \rightarrow U_4$

- b) Evaluating the paths path 3 can be neglected

$$\tau = \tau_{CQ} + \tau_{CL} + \tau_{Su}$$

For path 1 $\tau_1 = 1.5 + 0.15(2) + 0.2 \times 2 + 0.2 + 0.05(2+1) + 0.14 \times 2 + 1 = 3.83 \text{ ns}$

Path 2 $\tau_2 = 1.5 + 0.15(1.5+2) + 0.2 \times 2 + 0.4 + 0.12 \times 2 + 0.18 + 1 = 4.24 \text{ ns}$

So path 2 is the critical path $\tau_{max} = 4.245$
 $f_{max} = 236 \text{ MHz}$

- c) For K input of FF-45 the path is path 1 $U_4 \rightarrow U_3 \rightarrow U_5$

$$\text{Set up time slack} = T_{required} - T_{arrival}$$

$$T_{required} = T_{max} - T_{su} = 4.245 - 1 = 3.245 \text{ ns}$$

$$T_{arrival} = \tau_{CQ} + \tau_{CL} = 1.5 + 0.15 \times 2 + 0.2 \times 2 + 0.2 + 0.05(2+1) + 0.14 \times 2 = 2.83 \text{ ns}$$

$$T_{\text{set up slack}} = 3.245 - 2.83 = 0.415 \text{ ns}$$

or $= 0.615$ if fan-out output neglected

$$\text{hold time slack} = \tau_{arrival} - \tau_{hold} = 2.83 - 0.5 = 2.33$$

No violation

or $= 2.13$
 if fan-out of output is neglected

Q5

a) Two paths
D4 - U3 - D5
D5 - U2 - D4

$$\left. \begin{aligned} \text{Path 1} & \cdot 2 + 0.45 * 3 + 0.4 + 0.35 * 4 = 5.15 \text{ ns} \\ \text{Path 2} & \cdot 2 + 0.45 * 1 + 0.2 + 0.15 * 4 = 3.25 \text{ ns} \end{aligned} \right\}$$

$$\text{Arrival at Point F} = \text{Delay of D4} = t_{CQ} + t_{CL} + \text{Fanout} = \underline{3.35}$$

$$\begin{aligned} \text{Required time at F} & = 20 \text{ ns} - t_{su} - \text{Delay of U3} \\ & = 20 - 1 \text{ ns} - 1.8 \text{ ns} = \underline{17.20 \text{ ns}} \end{aligned}$$

$$\text{Slack time at F} = 17.20 - 3.35 = \underline{13.85 \text{ ns}}$$

b) Path 1 is the critical path D4 - U3 - D5

$$T_{i \text{ max}} = T_{CL} + T_{CL} + T_{CQ} = 5.15 + 1 = 6.15 \text{ ns}$$

$$\text{Temp effed, } k_t = \left(\frac{T_J - 25^\circ \text{C}}{30^\circ \text{C/W}} \right)^{1.5} = \left(\frac{273 + 70}{273 + 25} \right) = \left(\frac{343}{298} \right)^{1.5} = \underline{1.235}$$

$$\text{Voltage effed } k_v = \frac{1}{1 - 0.05} = \underline{1.0526}$$

$$K = k_t * k_v = 1.235 * 1.0526 \approx \underline{1.3}$$

$$\text{Overall Delay} = K * T_{i \text{ max}} = 1.3 * 6.15 \approx \underline{8 \text{ ns}}$$

$$\text{Worst case frequency, } f = \frac{1}{8 \text{ ns}} = 125 \text{ MHz}$$

Question 6 P1

Assume the following decoding

x y
 0 0 $x = y$
 0 1 $y > x$
 1 0 $x > y$
 1 1 X

A_{i+1}	B_{i+1}	x	y	A_i	B_i
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	1	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	0	0

$A_{i+1} B_{i+1}$

x	y	00	01	10	11
0	0	0	0	X	1
0	1	0	X	1	0
1	0	1	X	1	0
1	1	1	X	1	0

$A_i B_i$

x	y	00	01	10	11
0	0	0	1	X	0
0	1	1	1	X	0
1	0	3	1	X	0
1	1	2	1	X	0

$A_i = A_{i+1} + \bar{B}_{i+1} x \bar{y}$

$B_i = B_{i+1} + \bar{A}_{i+1} \bar{x} y$

Now that we have the Boolean expression for A_i & B_i we can proceed and the VHDL code for the bit comparator and the easiest would be a behavioral description.

```

library IEEE;
use IEEE STD_LOGIC_1164.ALL; -- other use statements of STD library if needed
entity Component_1 is
    Port (A_in, B_in, x, y: in std_logic; A_o, B_o: out std_logic);
end Component_1
architecture behavioral of Component_1 is
begin
    process (A_in, B_in, x, y)
    begin
        if (A_in = '1' and B_in = '0') then A_o <= '1'; B_o <= '0';
        elsif (A_in = '0' and B_in = '1') then A_o <= '0'; B_o <= '1';
        elsif (x = '1' and y = '1') then A_o <= '0'; B_o <= '0';
        else A_o <= x; B_o <= y;
        end if;
    end process;
end behavioral;
    
```

COEN 6501 Dec 12, 2015

Question 6 - Continued P2

-- library statements here ..

entity Component_8 is

Port (Ain, Bin : in std_logic;
x, y : in std_logic_vector 7 downto 0); A0, B0 : out std_logic);

end Component_8;

architecture structural of Component_8 is

Component_1

Port (Ain, Bin, x, y : in std_logic; A0, B0 : out std_logic);
end Component_1

signal sa, sb : std_logic_vector(7 downto 0);

begin

for com7 : Comparator_1 use entity work Comparator_1 (behavioral);
comp7 : Comparator_1 portmap (Ain, Bin, x(7), y(7), sa(7), sb(7));

for comp6-1 : Comparator_1 use entity work Comparator_1 (behavioral);

stages: for i in 6 downto 1 generate

comp*i*-1 : Comparator_1 portmap (sa(i+1), sb(i+1), x(i), y(i), sa(i), sb(i));

end generate;

comp0 : Comparator_1 portmap (sa(1), sb(1), x(0), y(0), A0, B0);

end structural;