Department of Electrical and Computer Engineering
COEN 6501 Dec. 9, 2013

Answer all Questions. All Questions carry equal marks
Exam Duration 3 hour
No books or papers are allowed. Lecturer: Asim J. Al-Khalili

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Question 1

a) Discuss the merits of implementing digital circuits in FPGAs
b) Implement function F1 using 2, 3, and 4 variable LUT and select optimum implementation according to Table 1

F(A,B,C,D,E,F,G,H) = ABC + A'BE + BCFGH + CD'FH + AC'F'G

Table 1

Table Size, variables	Delay, ns	Area, mm^2
2	2	7
3	3	11
4	4	26

Question 2

Design the ***fastest circuit*** to implement the following function:

F = **X** Y – Z

where X and Y are 4-bit unsigned binary number and Z is 4-bit signed (2's complement) binary number:

X = $x_3\ x_2\ x_1\ x_0$, Y= $y_3\ y_2\ y_1\ y_0$, Z = $z_3\ z_2\ z_1\ z_0$

Identify the critical path and give estimated time in terms of full adders delay, T_f.

Question 3

Design a 4-bit ring counter with the following output: 0001, 1000, 0100,0010, 0001, 1000 and so on… Start with a state diagram and follow sequential circuit design procedure. Use D Flip Flop for your implementation.

Question 4

a. Determine the maximum speed of operation at typical conditions for the serial multiplier control circuit shown in Fig. 1, taking into consideration the fan-out loading only. Timing parameters for all components are listed Table.2.
b. At the maximum speed of operation, determine the slack time for the setup time and hold time at the D-input of Flip-Flop U6.
c. After the realization of the circuit on a silicon chip, a delay of 3.5ns has been introduced at the clock of U1 F/F relative to other clock signals. Calculate the maximum speed of operation.

Note: All inputs: Begin, Qo and Co have arrival time at $t = -\infty$.

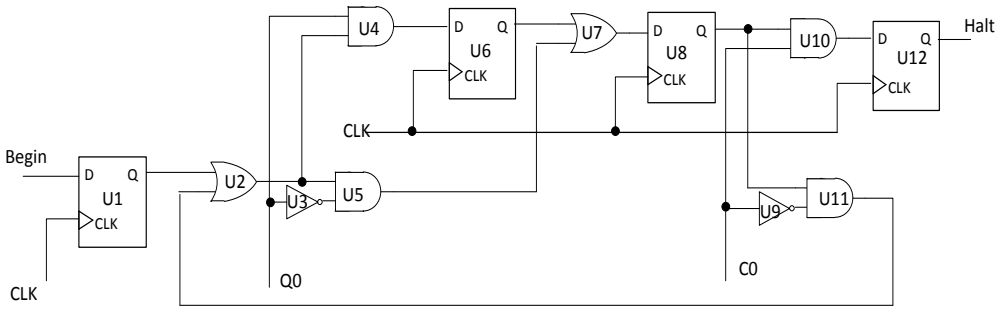

Fig. 1

Table 2

Component	Tp (ns)	Input Loading(UL)	K1 (ns/UL)
Inverter	1.5	1	0.2
2 input AND	2.0	1.5	0.25
2 input OR	2.5	1.5	0.25
D-F/F*	3.0	1 (all inputs)	0.2

* t_{su}=1.5ns, t_h=0.5ns

Question 5

The circuit shown in Fig. 2 operates in the military temperature range of -55°C to 125°C with a supply voltage fluctuation of +/- 10%. The device is packaged in a flat pack with a thermal resistance of 30°C/W and dissipates power of 3W. The input signals, A, B and C arrive at t =0.

The timing characteristics of each of the components of the circuit are shown in Table 3.

a. Determine the worst case arrival time of signal A at point D

b. Determine the maximum clock frequency of operation to guarantee reliable operation.

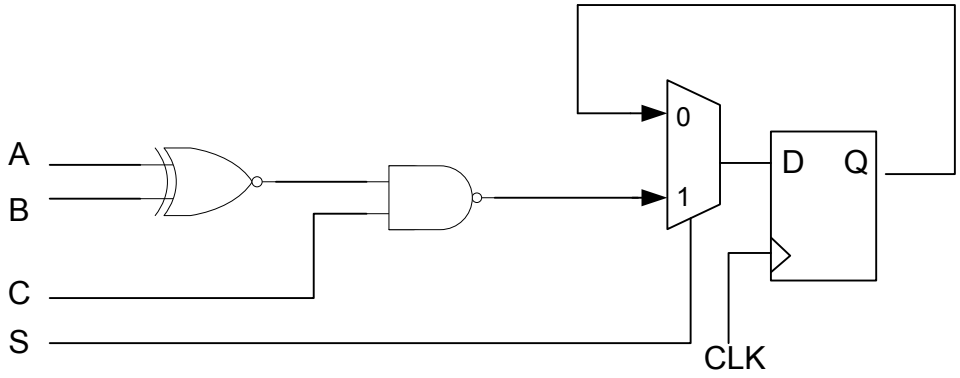

Fig. 2

Table 3- Timing Characteristics of Logic Gates

Gate	Intrinsic delay Tp (ns)	Input Loading (UL)	K1 (ns/UL)
2 input NAND	0.25	2	0.03
2 input XNOR	0.4	2	0.05
2 input Mux	0.3	1.5	0.1
D Flip-Flop (TCQ) Tsu=0.2ns, th=0.1ns	0.5	2	0.07

Equations

$$T_d = \left(T_p + K_1 \sum N_i + K_2 M_L\right) \times K^* \qquad K^* = K_T \times K_V \times K_P$$

$$K_T = \left(\frac{T_2}{T_1}\right)^M, \; t_j = t_a + \Theta_{ja} \times P_d, \quad \text{M=-1.5}$$

$$K_V = \frac{1}{1 + 0.01 \times f_s} \qquad K_P = 1 + 0.01 \times f_P$$

Question 6

a) Write a VHDL Code that represent the following circuit given in Fig. 3

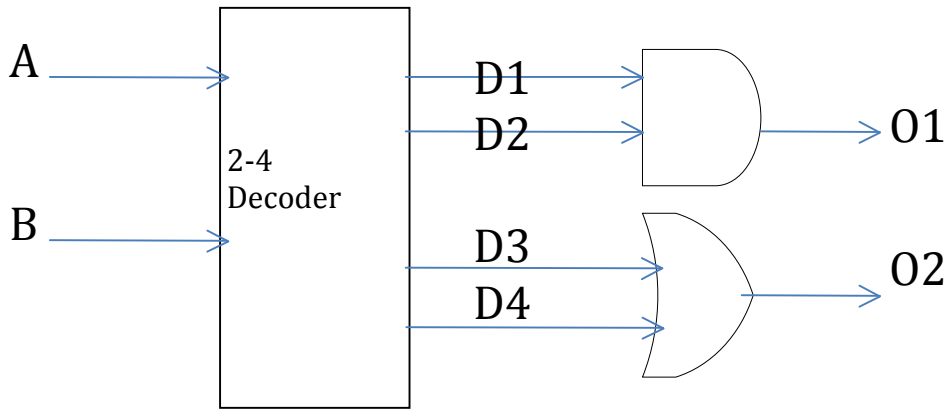

Fig. 3

b) Find the Syntax and Semantic errors in the code below:

```
entity H_A_Con is   ............................. L1
port (X,Y:Istd_logic;.............................L2
         SUM,CARRY:out std_logic);.......  .......L3
end Half_A_Con;    ...............................L4
architecture behavioral of H_A_Behav is ..........L5
--signal X,Y:integer;  ...........................L6
-signal SUM,CARRY:bit; ...........................L7
begin
     process (X,Y); ..............................L8
     variable Z:integer; ..........................L9
     begin   .....................................L10
          SUM<='0';  .............................L11
          CARRY<='0'; ............................L12
          Z:=X+Y;  ...............................L13
          if (Z=1) then SUM<='1';  ..........    ..L14
elsif (Z=2) then CARRY<='1';   ..................L15
          end ;   ................................L17
     end process;   ..............................L18
end behavioral;      .............................L19
```