Structured ASIC, Evolution or Revolution?

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ABSTRACT

This paper describes the structured ASIC technology and impacts to the implementation flow. With an optimized and programmable structure, the structured ASIC technology indeed introduces a dramatically reduce ASIC cost and manufacturing turn-around time. While, the structured ASIC implementation flow is more complex than the conventional cell-based flow. There would be slightly impacts to structured ASIC implementation problems. Finally, the structured ASIC solutions provided by Faraday would be given. There are 3 structured ASIC solutions for customers' different applications. The three solutions are MPCA (Metal programmable Cell Array), MPIO (Metal Programmable I/O), and the structured ASIC platform. With the most competitive architecture, our customers can implement their ASIC at a lower cost with a faster turn-around-time.

Categories and Subject Descriptors

B.7. [**Integrated Circuits**]

General Terms

Design

Keywords

Structured ASIC; ASIC;

1. INTRODUCTION

Shrinking process technology migration to very deep submicron, increasing chip complexity, more complicated verification tasks, but shorter time-to-market have multiplied the difficulty of designing systems-on-a-chip (SOC) in the deep submicron era. Moreover, the non-recurring engineering (NRE) cost, including implementation engineering effort and mask tooling charges, increases significantly as the process technology migration. The NRE cost is too expensive for all but the very high volume applications (quarter million plus units per year). And time-to-market pressure, frequent feature changes and product derivatives further exacerbate the cost issues. A new breed of ASIC products,

called "Structured ASIC", can cut NRE expenses by more than 90% for derivative chips, and speedup the time-to-market. As a result, the structured ASIC is becoming imperative for deep submicron designs.

Table 1 is a cost comparison between typical 1-million-gate design 0.13μm process for FPGA, structured ASIC and cell-based ASIC implementations.

Table 1: FPGA, structured ASIC, and cell-based ASIC development costs

	FPGA	Structured ASIC	Cell-based ASIC
Total Design Cost	$165K	$500K	$5.5M
Vendor NRE	None	$100K~$200K	$1M~$3M
Cost of EDA Tools	$30K	$120K~$250K	> $300K
Man Power	1 to 2	2 to 3	5 to 7
Price per Chip	$200 ~ $1K	$30 ~ $150	$30
Unit Cost (Qty 1K)	$1000	$500~$650	$55K
Unit Cost (Qty 5K)	$220	$110~$150	$1.1K
Unit Cost (Qty 500K)	$40	$21	$11
Source: Semiview, December 2003			

FPGA-based products uniquely address the economic issues for lower volume applications by being easy to design and program within the shortest possible time. However, FPGAs consume more power, are much lower in performance, and come with substantially higher units costs when compare to cell-based ASIC. In other words, FPGAs are unsuitable for certain higher performance, higher volume applications, or those applications with low-power requirements that are best met with cell-based ASIC technology.

On the other hand, when compared with cell-based ASICs, Structured ASICs offer shorter turn-around-time, and required less NRE charges for future functional changes. Structured ASIC technology is especially suitable for platform ASIC designs that have integrated most of the IP blocks and leave some space for customer function changes or bugs fixing in the future.

A structured ASIC is different from the traditional cell-based ASIC. It contains an array of well-structured and optimized elements across the entire chip. The structured element is designed for implementing the desired functional by making changes to fewer upper layer mask. The structured ASIC

technology can save significant amount of NRE cost and time-to-market.

The implementation flow of structured ASICs involves mainly 6 steps, which include logical synthesis, DFT insertion, placement, physical synthesis, clock tree synthesis and routing. Implementation problems in structured ASICs are little complex than the problems in other design styles. These problems mainly depend on the structured ASIC architecture in which the circuit has to be implemented. The conventional algorithms for general FPGA or cell-based can be modified for the implementation in structured ASICs.

The rest of the paper will be organized as follows. Section 2 describes the structured ASIC technology and its advantages and disadvantages. Section 3 shows the implementation flow for structured ASICs. Section 4 gives a brief introduction to Faraday structured ASIC solutions and implementation flow. The concluding remarks follow in Section 5.

2. STRUCTED ASIC TECHNOLOGY

2.1 The Architectures of Structured ASICs

The structured ASIC architecture mainly consists of two parts: the structured element, and the array of structured element. The general architecture of structured ASIC contains an array of structured elements. The structured element is similar to the gate array due to its well-structured nature. Gate array also contains many of gates across the entire chip. This gate is basically an array of uncommitted MOS transistors. The difference between gate array and structured ASIC is that the structured ASIC offers an array of partially formed elements. These elements are fully optimized in terms of area and performance. The structured element is also similar to the FPGA programmable element but does not have the additional overhead required for field programmability.

There may exist one or more types of structured elements in the chip. These different types of elements form the array in the Structured ASIC. Each type of elements is activated for different purposes. For example, one type of element is for combination logic, and another type is for sequential element. Figure 1 illustrates the general architecture of the structured ASIC. There are 2 types of structured element. The first one is the logical element, and the other is the storage element. The different structured elements can be different or the same size.
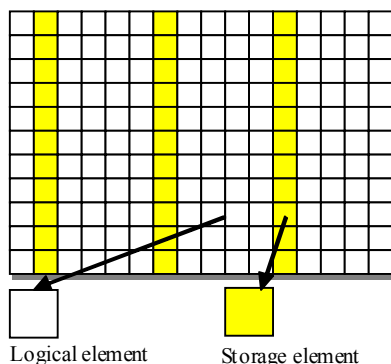

Figure 1: The structured ASIC general architecture

There are 2 types of structured elements. The first type is based on look-up tables, while the second is based on transmission gate.

■   Look-up table style

Each structured element is designed as look-up table to implement logical function. The look-up table architecture is widely used in FPAG logic block design. The structured element can be programmed any n-input logical function, where n is the inputs of the structured element. Typically, the value of n is less than 5 for the circuit performance issue.

■   Transmission gate style

Each structured element implements the logical function from generic transmission gates. Disadvantages to use transmission gate style are the restricted provided logical function in comparison with look-up table style. On the other hand, the transmission gate style can provide a substantially lower performance unit cost.

There are 2 models of array: the uniform and the non-uniform array styles.

■   Uniform array model

The uniform array model is setup as a regular grid array over the entire chip. There is one type of the structured element. That is, the structured element can be programmed as a logical element and sequential element. A typical uniform array is shown in Figure 2. All structured elements are uniform.
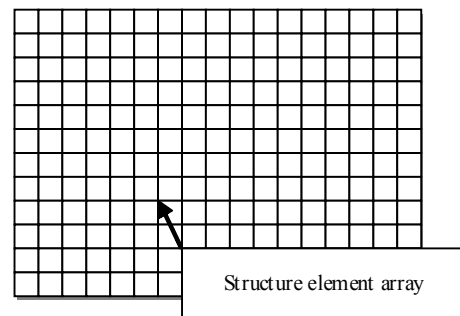

Figure 2: Uniform array model

■   Non-uniform array model

In non-uniform model, there are two more types of the structured element. Each type element has to be allocated on the specific locations on the chip. The specific locations have to be designed before the structured ASIC implementation. Figure 3 shows a typical non-uniform array model. There are 3 types of structured elements: FE, BUF and FF. The ratio of the number of different types is 4:2:1. The FE element is for logical function implementation, BUF element is a buffer for timing optimization, and FF element is for sequential function.
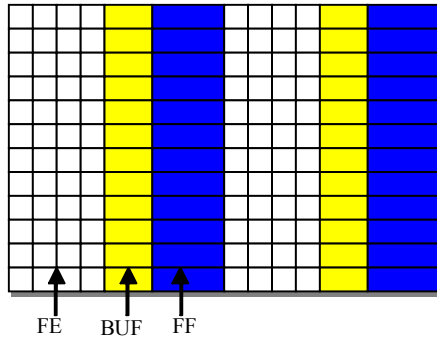
FE   BUF   FF

Figure 3: Non-uniform array model

2.2 The Advantages/Disadvantages

The major benefits of structured ASIC are listed as follows:

■ Shorten time-to-market

It usually takes about 2 to 4 tape-outs before mass-production, and each tape-out takes an average about 2 months for mask changes, fabrication and packaging. Use of structured ASIC can speed up that process. Average, we can save the "Time-to-Market" by 4 to 6 months.

■ Cut down the cost for bug fixed

Mask charges is growing exponentially – estimated at US\$600,000 for 0.13μm and US\$1,500,000 for 90nm, not a lot of companies can afford full mask change for bug fixes. Structured ASIC can cut down more than 90% of that mask charge for each additional tape-out.

■ Enable SOC platform design

In addition to the logical cells, SOC platform contain high-performance SRAM, ROM and other analog IP. Customer just uses structured ASIC as the customized logic blocks for the different applications to further cut down production time.

The major disadvantages of structured ASIC are listed as follows:

■ Chip area/performance overhead

The area per unit gate would be 3 to 1.5 times in comparison with the conventional standard cell design; the average performance degrade would be 10% to 50%. It depends on the architectures.

■ Customize EDA tools for specific structured ASIC architectures

Due to different structured ASIC architectures, a few EDA tools should be customized to offer a better and quick quality for structured ASICs

3. The IMPLEMENTATION FLOW FOR STRUCTURED ASIC

The implementation flow for structured ASICs involves mainly 6 steps, which include logical synthesis, DFT insertion, placement, physical synthesis, clock tree synthesis and routing. Figure 4 shows the structured ASIC implementation flow. The logical synthesis, which maps RTL design into structured elements, is the first step. DFT insertion adds the scan circuitry to improve the testability and fault coverage. Placement involves the mapping the smaller structured elements onto array elements. Physical synthesis improves the timing by placement-based optimization. Clock tree synthesis distributes the clock network to minimize the clock skew and delay. The final step is the routing.
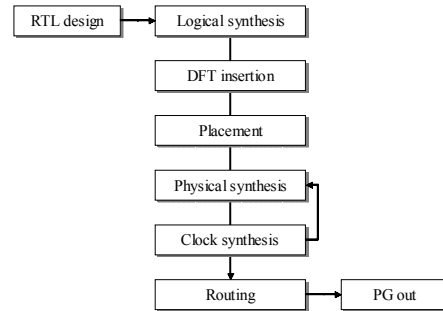

Figure 4: Implementation flow of structured ASICs

Logical synthesis, placement and routing problems in structured ASICs are slightly more complex than logical synthesis problems in other design styles. The other DFT insertion, physical synthesis and clock tree synthesis problems are the similar to the conventional ones.

The synthesis algorithms for general cell-based or FPGA are normally used for the synthesis. The problems mainly depend on the target structure element architecture. Placement problem in structured ASICs is very similar to the gate array or standard cell placement problem. The problems mainly depend on the target structured ASIC array architecture. The routing problem in structured ASICs is to complete the connection with the limited routing layers constraints. The constraint on the routing layers is the key for the reduction on mask NRE cost and manufacturing turn-around-time.

The structured ASICs DFT insertion, physical synthesis and clock tree synthesis are the same as the flows in the conventional cell-based ASIC. The only issue is that the completeness of the target structured ASIC library. Does the library provide scan flip-flop for each storage element? Are there enough cell types for physical synthesis? Are there enough clock buffer types for clock tree synthesis?

4. FARADAY STRUCTURED ASIC SOLUTIONS AND FLOWS

The structured ASIC technologies developed by Faraday include:

■ Metal programmable Cell Array (MPCA)

■ Metal programmable I/O (MPIO)

■ Application-oriented platform solutions

Faraday goal is to provide the most competitive element structures, with high performance, high density and low power consumption, while offering our customers a quick development environment, to build their ASIC at a lower NRE cost with a faster turn-around-time.

MPCA cell library is optimized for deep sub-micron designs with a focus optimizing routability, speed and minimizing power consumption. As shown in Figure 5, only the three metal layers are needed to program the library cells as well as place and route design.
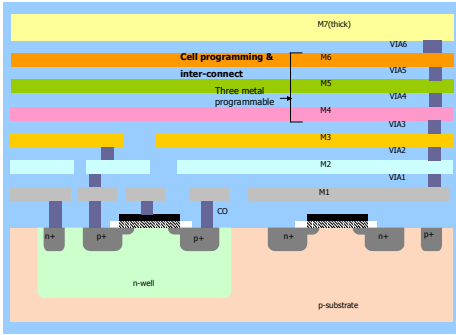
Figure 5: Programming layers for 1P7M process

By changing just one top metal mask, MPIO can support PCI33, PCI66, PCIX, SSTL2 class I/II, CMOS, and TTL I/O with different drive strengths and slew rate controls. Figure 6 is a block diagram of Faraday's MPIO.
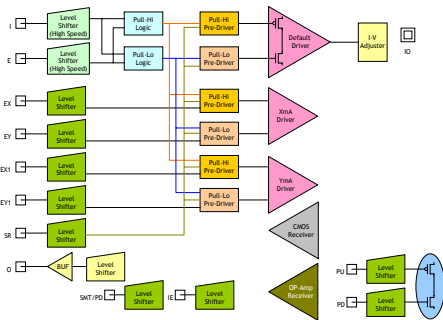

Figure 6: Block diagram of metal-programmable I/O (MPIO)

A structured ASIC based platform typically includes standard cell, embedded CPU and DSP, embedded memories, PLL, DLL or other analog IPs. Besides these silicon proven IPs, the remaining area of a platform chip is reserved for user-defined logics which can be easily modified at anytime in the future, with just three metal layer changes. Figure 7 shows the block diagram and layout view of the TFT/LCD platform chip co-developed by Faraday and a customer, where the MPCA block can be configured to work with different display systems.

The proposed structured ASIC implementation flow is exactly the same as the conventional cell-based ASIC flow because of Faraday competitive structured ASIC architectures. Moreover, Faraday has provided the structured ASIC logical synthesis, simulation, DFT synthesis, physical synthesis libraries compatible with existing commercial EDA tools [1][2][3]. Our customers can

implement their own chip by Faraday structured ASIC in the same cell-based flow, and do not have to purchase any new EDA tools.
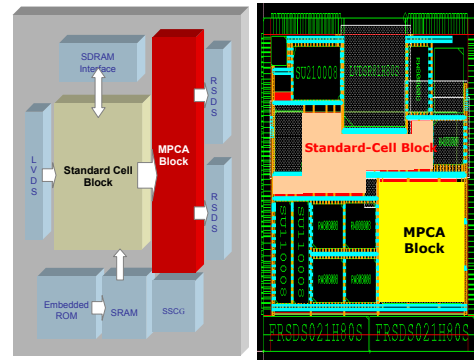

Figure 7: Block diagram and layout view of Faraday's TFT/LCD platform

5. CONCLUSION

The structured ASIC technology is being used as a new approach to ASIC designs, which can cut down NRE cost, and also offer a impressive reduction in time-to-market. The structured ASIC technology architecture mainly consists of two parts: the structured element and the structured element array. Due to the structured ASIC architecture, there would be slight impacts to the traditional cell-based ASIC implementation flow. According to different architecture, some of EDA tools should be enhanced to achieve a better performance result. Faraday has proposed 3 structured ASIC solutions: MPCA, MPIO and application oriented platform based solution. With the competitive technology architecture, our customers can realize their ASIC design by their conventional cell-based ASIC implementation flow. Is structured ASIC a revolution or evolution? Both are yes. The structured ASIC is a revolution to ASIC business, but is just another evolution of ASIC implementation.

6. REFERENCES

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[3] Synopsys Design Compiler *User's Guide and Document Reference Manual.* 2003.