

EE 4743 Test #1 Solutions - Fall 1999 – Reese

1.
 - a. Maximum Register to Register delay
 $tcq + T_{prop\ reg2reg\ max} + Tsu = 3 + (G5+G2+G1+G3) + 2ns = 3 + 16 + 2 = 21\ ns$
 - b. Maximum clock to out delay
 $clk\ buff + Tcq + max\ prop\ to\ out = I3 + tcq + (G5+G1+G1+G4+I5) = 5 + 3 + 21 = 29\ ns$
 - c. Maximum pin to pin delay (that is not clock to out delay)
 $I2 + G2 + G1 + G4 + I5 = 5 + 12 + 5 = 22ns$
 - d. Setup time on B input
 $B\ max\ prop\ to\ D + Tsu - Clk\ Min\ prop = (I1 + G2 + G1 + G3) + Tsu - I3 = 5+ 12 + 2 - 5 = 14\ ns$
 - e. Hold time on B input
 $Clock\ Max\ prop + Thd - B\ min\ prop = I3 + Thd - (I1 + G2) = 5 + 1 - (5 + 4) = -3\ ns$

2. (20 pts) See Figure.

3. (20 pts)

architecture a of Fminus is

```
begin
  process (din)
  begin
    dout(7 downto 0) <= not din(7 downto 0); -- assume 0.0 < din < 1.0
    dout(8) <= '0'; --- sign must be zero! Cannot complement Sign bit!!!!
    if (din(8) = '1') then
      dout <= "000000000"; --- 0.0, assign all 9 bits
    elsif (din = "000000000") then
      dout <= "100000000"; -- 1.0, assign all 9 bits
    end if;
  end process;
end a;
```

4. Write the truth table for the combinational functional below that is described by the VHDL process.

A	Y0	Y1
0	1	0
1	0	1

5. See notes for Ripple carry adder structure.

6. 32 x 2

7. Monolithic SRAMs are more area efficient (LUTs are spread out with routing between LUTs), are faster (address decode logic is optimized , also routing area is smaller, more optimized).

8. Wafers with transistors are pre-fabricated; only have to create final routing layers.

9. In case of overflow, gives answer that is closer to correct answer (saturated adder: $255 + 1 = 255$, normal 8 bit adder: $255 + 1 = 0$).
10. Removes skew between internal, external clocks; clock multiplication and division.
11. Clock 2 Out of FPGA #1, External Setup time of FPGA #
12. Place a DFF as close as possible to the input with no intervening logic.
13. Number of clock cycles between when an Input is applied to when the output value is ready.
14. External Hold Time.