EE 3714 Test #4 Solutions- Spring 2000 – Reese

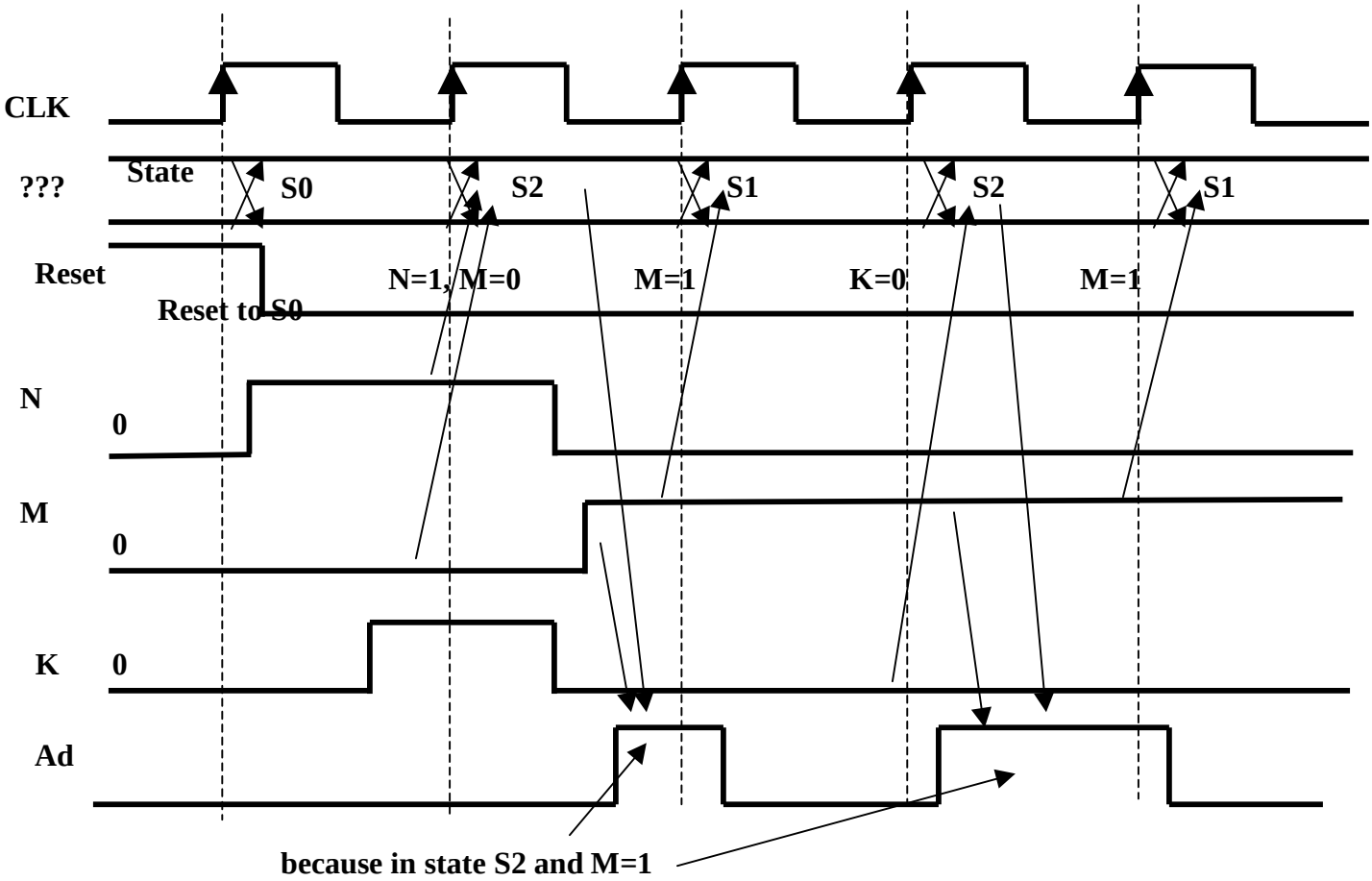
Work all problems.

1. (15 pts) For the ASM chart in Figure #1 (Figure 22-10, pg 575, book), the state encoding is one-hot using S0=001, S1=010, S2=100.

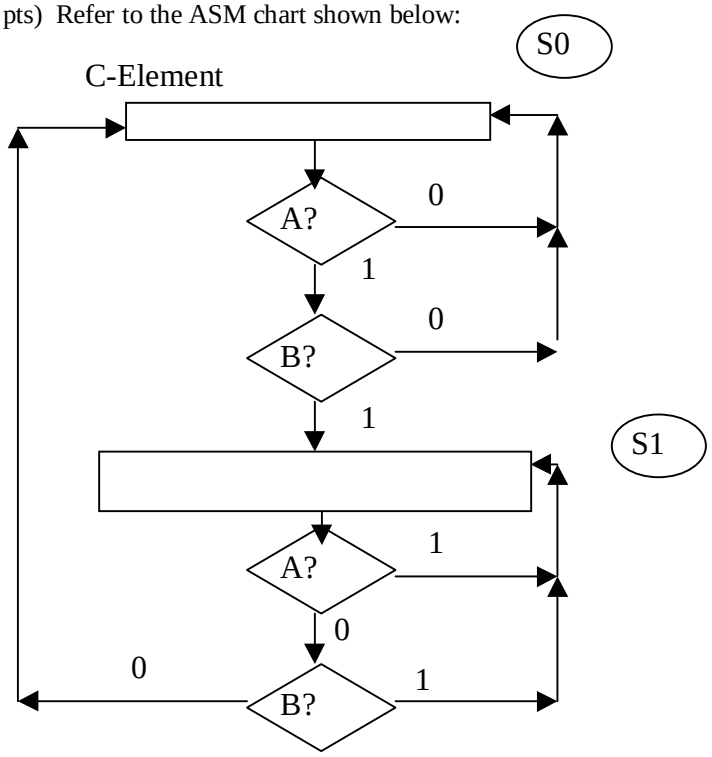
   a. Write the boolean equation for the D2 input (D input for state S2 D-Flip-flop)
   *D2 = Q0 N M' + Q2 M'K' + Q1 K'*

   b. Write the boolean equation for the "Ad" output.
   *Ad = Q2 M + Q0 N M*

2. ( 15 pts) For the ASM chart in Figure #1, complete the timing diagram below for the State and "Ad" waveforms. Assume that rising edge triggered DFFs are used for the FSM implementation. Make sure you complete the waveforms for State, Ad through the last clock cycle.



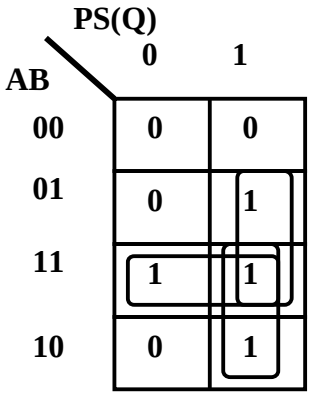
3. (20 pts) Refer to the ASM chart shown below:

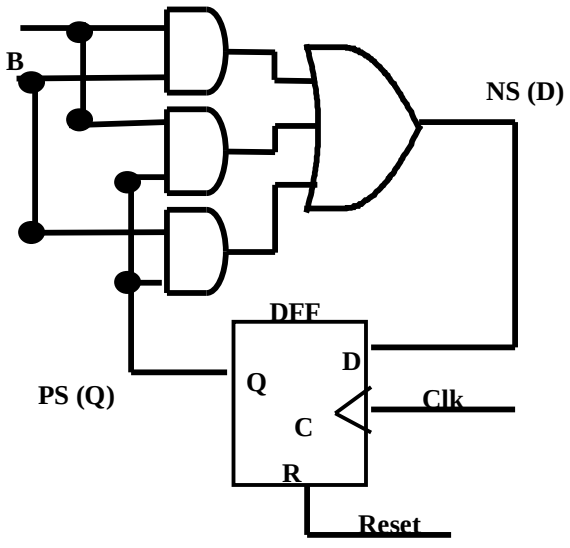



Assume the implementation uses one D-FF, and the state encoding is S0=0, S1=1. Complete the state table below, and draw the implementation of this digital system (show the DFF plus combinational gates that implement the ASM chart. Use an asychronous reset in your design to reset to state S0.

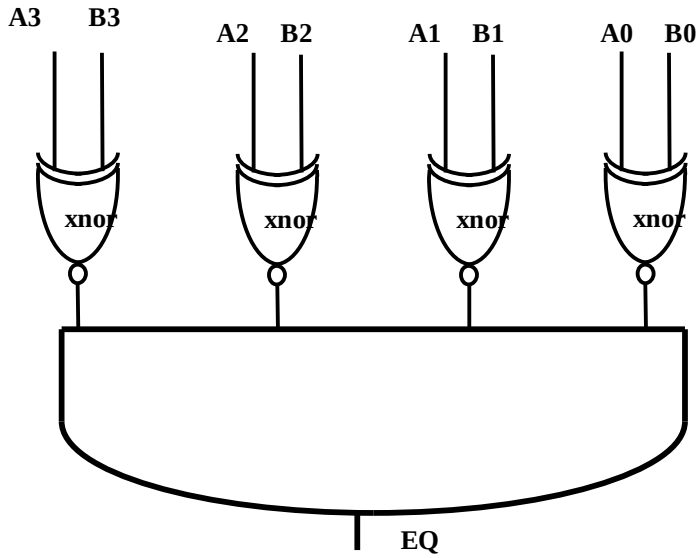
| PS | A | B | NS |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**D = AB + QB + QA**

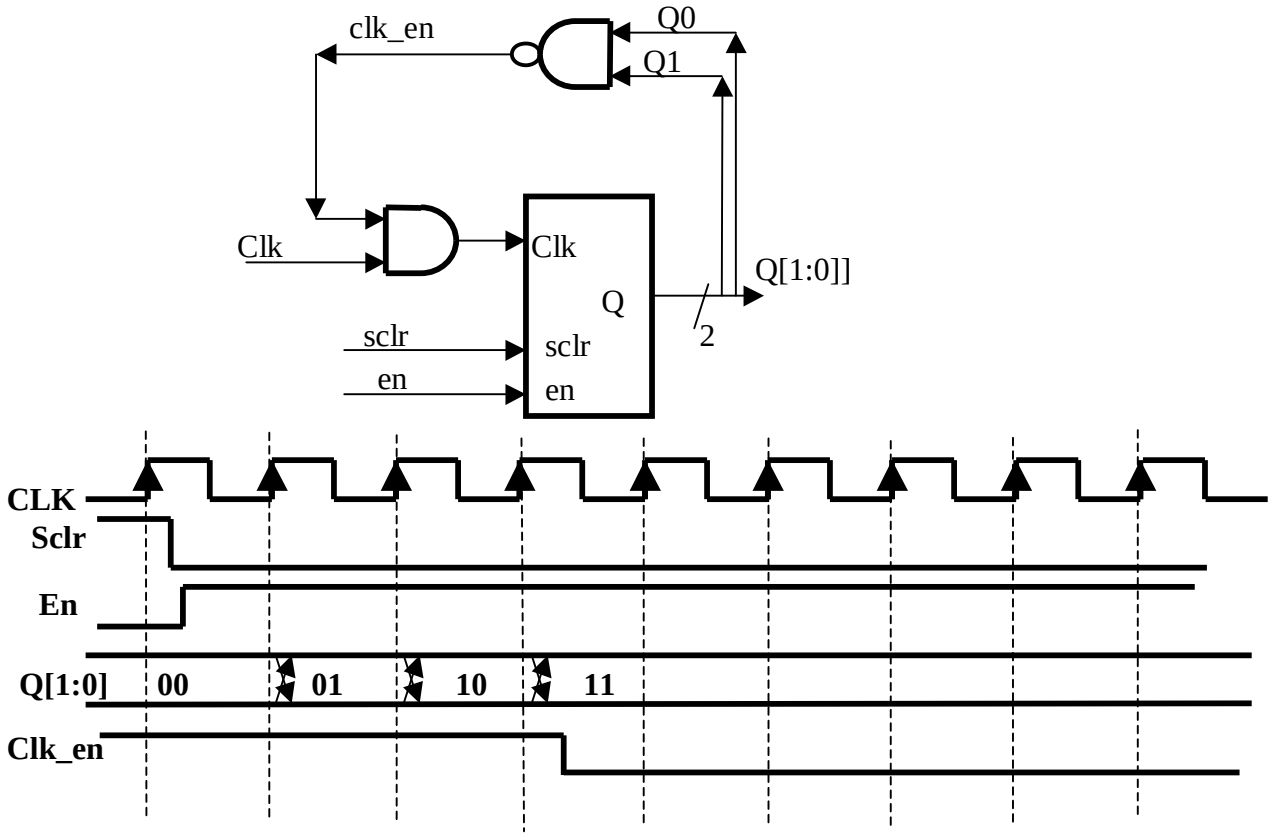


4. (10 pts).
Draw the gate level diagram of a 4-bit comparator circuit (Eq <= '1' when (A = B) else '0').




5. (15 pts) The schematic below shows a sequential system with a 2-bit binary counter. Complete the timing diagram below for the Q output and 'clk_en' signals. The EN input to the counter enables counting, the SCLR input is a synchronous clear. The counter is rising edge triggered.




When clk_en = '0', clk signal to counter = 0, so counter does not count.

6. (10 pts) Explain the difference between a complex PLD and an Field Programmable Gate Array. Draw diagrams to illustrate the difference.

*See notes for diagram. A Complex PLD has several PAL blocks with programmable routing between the blocks. An FPGA has a row-column arrangement of primitive logic element (anything that can implement a complete logic family like a 2-input Nand gate or 4 input lookup table) with programmable routing between the elements.*

*7.* (5 pts) Discuss two advantages for describing a circuit via VHDL rather than a schematic of gates.

*VHDL is more readable in terms of circuit behavior than a schematic, is easier to change, is more portable between different implementation techologies.*

8. (5 pts) What common combinational building block does the following VHDL statement describe??

Y <= A when (s = 1) else B

*This is a 2-to-1 mux .*

9. (5 pts) A sequential system can be broken into two parts-- combinational logic + memory. We also talked about dividing a sequential system into two parts by FUNCTION -- what was the terms we used for these functional parts of a sequential system???

*Control (FSM) + Datapath*