

## MaxPlus II Tutorial with Basic Graphical Gate Entry and Simulation

**Obtaining the MaxPlus Software:** The student version of the MaxPlus II software can be obtained directly from the Altera web site ([www.altera.com](http://www.altera.com)). After obtaining the software, you will have to obtain the licensing key from Altera and this is performed in the following manner:

1. Go to [http://www.altera.com/html/univ/student\\_edition/student-get.html](http://www.altera.com/html/univ/student_edition/student-get.html).
2. Select the “Download the MAX+PLUS II Student Edition software” link.
  - a) Select “I Agree” at the bottom of the page.
  - b) Select the “Download Student Edition software student923.exe (23,373,754 bytes)” to get the program. This will take some time.
  - c) Select the “Download software patch student923\_vhd.exe (601,665 bytes)” to get the software patch. (This patch has a compressed replacement for file vhd.d11.)
3. Continue to step 2 to apply for a license either (on the same page) by selecting the “Altera University Program: MAX+PLUS II Student Edition Licenses & Authorization Codes” link or go to <http://www.altera.com/maxplus2-student/index.html>.
  - a) Select “Version 9.23” (or the latest version available). Then select “Continue.”
  - b) Altera will now ask you for a hard disk number. You can get this from your PC by opening a DOS window and reading the disk volume number at the top when you type a DOS “dir” command.
  - c) Fill out Altera’s questionnaire and make sure you give them a valid email address. After you have filled out the questionnaire and clicked “Continue”, you will get a message saying that they will email a license file. Now click on the “ View the MAX+PLUS II Student Edition Installation Instructions” link. Follow the instructions there to install the software, install a patch, and setting up the licensing. You might want to save this or print it.
    - i) When you receive the license, install it in directory \max2work.
    - ii) Run MAX+plus II 9.23 Baseline.
    - iii) Choose License Setup (Options menu).
    - iv) Specify the license file by clicking Browse. In the Directories box, go to the directory in which you saved your license.dat file (e.g., c:\max2work), select the license.dat file in the Files box, and click OK.

**Example Problem:** Given the logic equation  $Y = A*B + /C$ , implement this equation using a two input AND gate, a two input OR gate and two inverters under the MaxPlusII environment. Upon completion of the schematic entry portion of the example, simulate the circuit and print out copies of the circuit & simulation results. Draw a Logic Table for the inputs & output and compare it with the simulation results.

### I. Circuit Design Tutorial

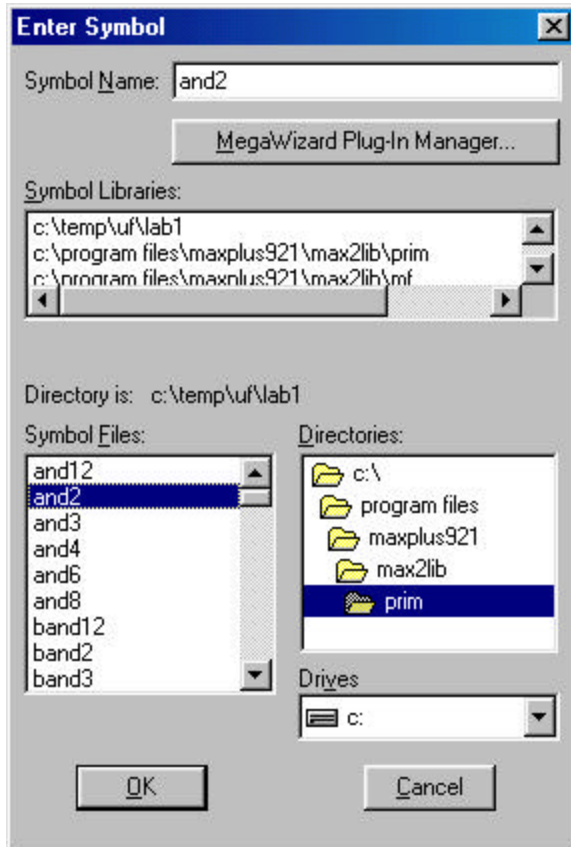
#### **A. New Design Creation**

1. Setup a ‘lab1’ directory on your PC to hold your design & simulation files.
2. Launch the Altera MaxPlus II software under Windows.
3. Select the pull-down button “MAX+plusII” and select “Graphic Editor”.
  - This should open a palette or circuit board that is designated “Untitled1- Graphic Editor”.
4. Select the pull-down button “file” and save the graphic design file “lab1.gdf” in your ‘lab1’ project directory created in step #1.
5. Select the pull-down button “file” again and select “Project” >> “set project to current file”. This tells the MaxPlusII application that this current design file is the one you wish to compile and simulate.

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### B. Component Selection Process

1. With your mouse pointing inside the palette, right click on your mouse and select “enter symbol”. A window listing the available Altera library component files should appear.
2. In the Symbol Libraries field, double click on the “..\max2lib\prim” library. This loads the “primitives” library and you should see several components listed in the “Symbol Files:” field.



3. Select “and2” and press the “ok” button. You should see a two input AND gate appear on your palette. Note: You may have to press the “+” magnifier (increase scale) on the left column of buttons to zoom in on the gate. In addition, try pressing the “-” magnifier to zoom out on the gate.
4. Repeat steps 1-3 to place an inverter on the palette. Note: The inverter is designated as a “not” in the Symbol Files field.
5. Place another inverter “not” gate on the palette. Finally, place a two-input OR gate “or2” on the palette.

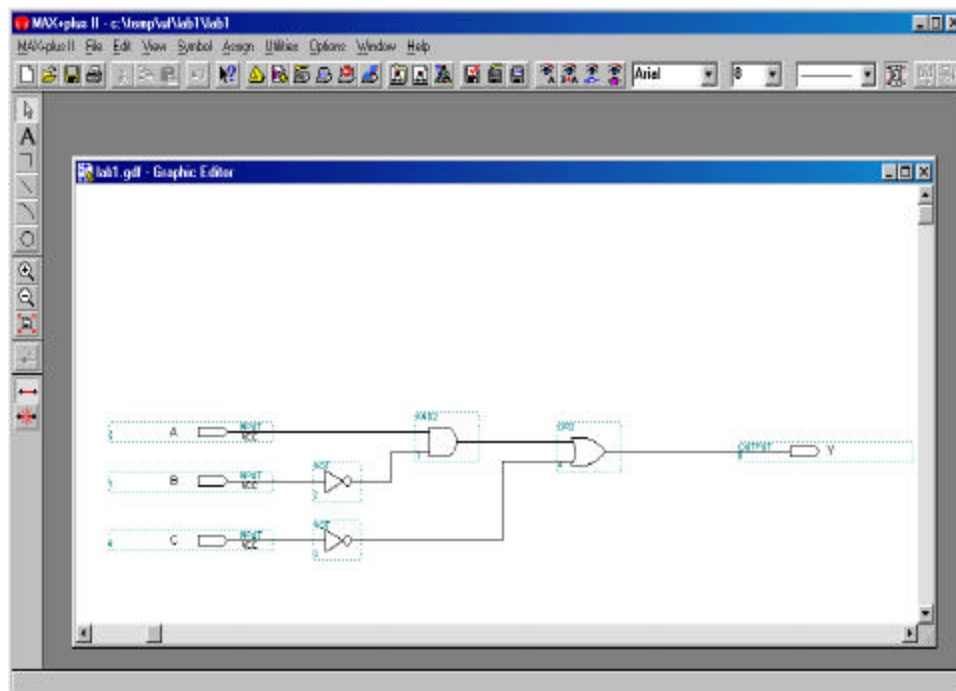
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### C. Adding/Deleting Wires & Moving Components

1. Place your pointer on the output of the inverter and hold the left mouse button down. You should see a cross-hairs or “+” appear at the output.
2. Drag your pointer to the input of the AND gate. Note: If you just create a single wire segment or two segments that do not connect to any gate, just place your pointer on the end of the open wire segment and drag it to the input of the gate.
3. To delete a wire, simply click on it (it should change color to indicate selection) and press the delete key.
4. Try moving a component by selecting it with your mouse, holding down the left button and moving it to another location on the palette. Note: If wires are connected to the component you move, they drag and stay connected to the component. This is referred to as ‘rubber banding’ and is a feature of all major schematic entry design packages.

### D. Adding Input & Output Ports

1. In the same manner that you placed a gate onto the palette, add an input port (designated “input”) from the Symbol Files list (Entry Symbol window).
2. Click on the input pin name (on the left of the input port symbol) and change it to ‘A’.
3. Repeat these two steps to create input ports ‘B’ & ‘C’.
3. In the same manner that you placed a gate onto the palette, add an output port (designated “output”) from the Symbol Files list (Entry Symbol window). Change the pin name to ‘Y’ on the output port.
4. Save your design. You are now ready to proceed to simulation of the circuit.



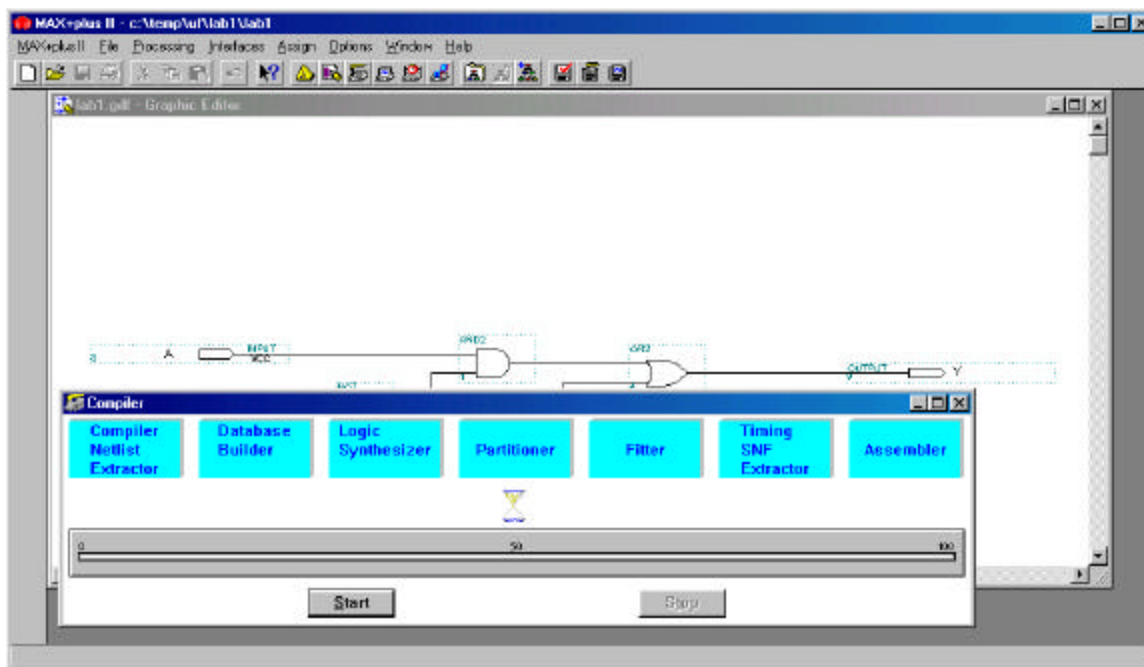
## II. Circuit Simulation

### A. *Fitting the Design to a Component*

1. After you have created the circuit, you need to make sure that you set the project to this current circuit as described in IA. New Design Creation, Step #5. For clarity purposes this is described again as:

Select the pull-down button “file” again and select “Project” >> “set project to current file”. This tells the MaxPlusII application that this current design file is the one you wish to compile and simulate.

2. Before we can simulate the design, we first must run the fitter software to place the design into a programmable component. Place your mouse over the icon on the top bar that has a small smokestack. On the bottom bar of the window you should see an icon help message saying “Opens the compiler window or brings it to the foreground”.
3. Press the smokestack icon (compiler) and the following compiler window should open up:



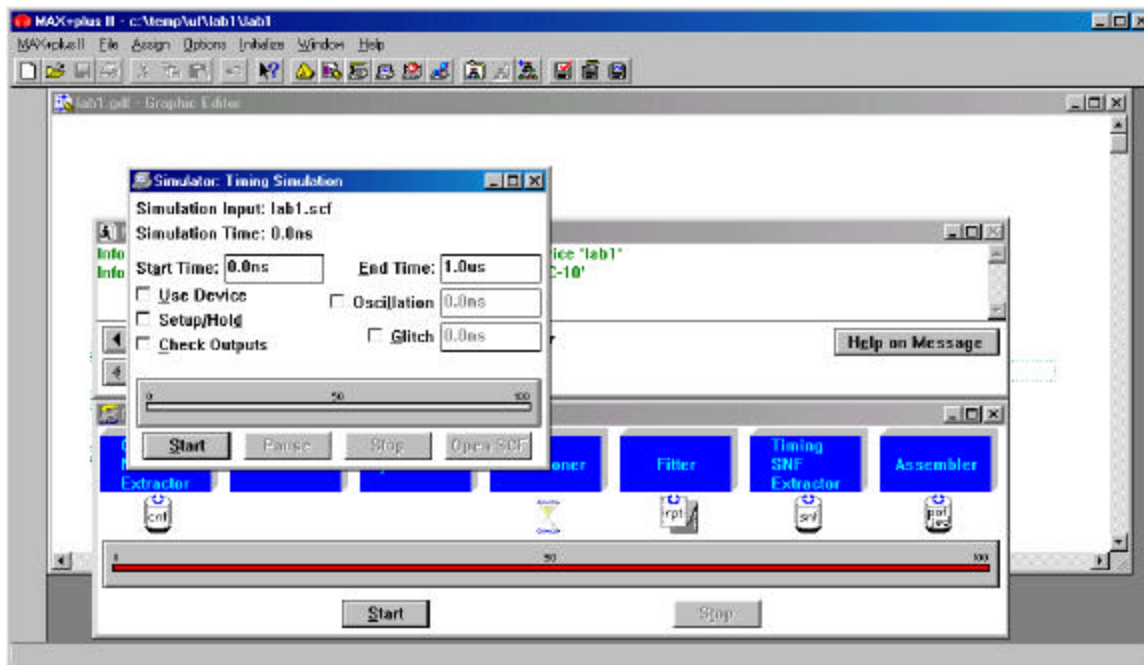
4. Press the start button in the compiler window. You should see a message back from the compiler that a device has been automatically selected from the “MAX7000” device family and that the design has been successfully fitted (placed) into this part.

**Special Note:** The compilation process consists of several sub-processes that we will breakdown and describe at a future date. For now, we just want you to understand the main function of the compiler is to translate the circuit into a set of equations that are fitted or placed into a programmable logic device.

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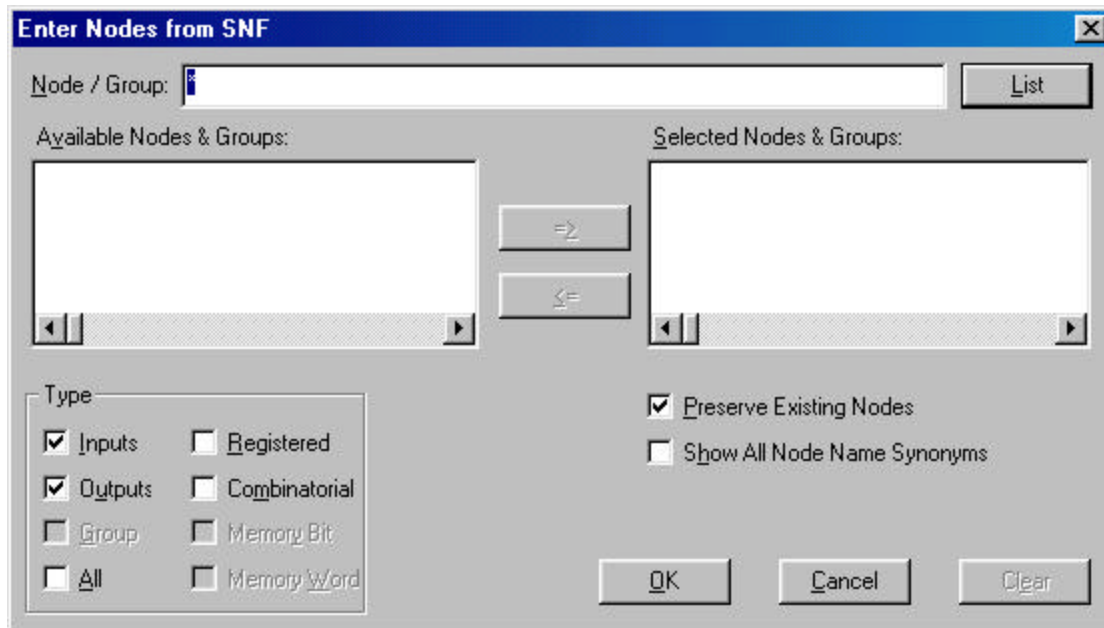
### B. Creating a Waveform for use with the Simulator

1. Once the circuit has been fitted into a particular programmable logic device, we now can run the simulator to check the circuit functionality. Place your mouse over the icon on the top bar that looks like a personal computer (next to the smokestack icon). You should see a icon message on the bottom of the MaxPlus window that says “Opens the simulator window or brings it to the foreground”.
2. Press the simulator icon and you should see the following simulation window open:

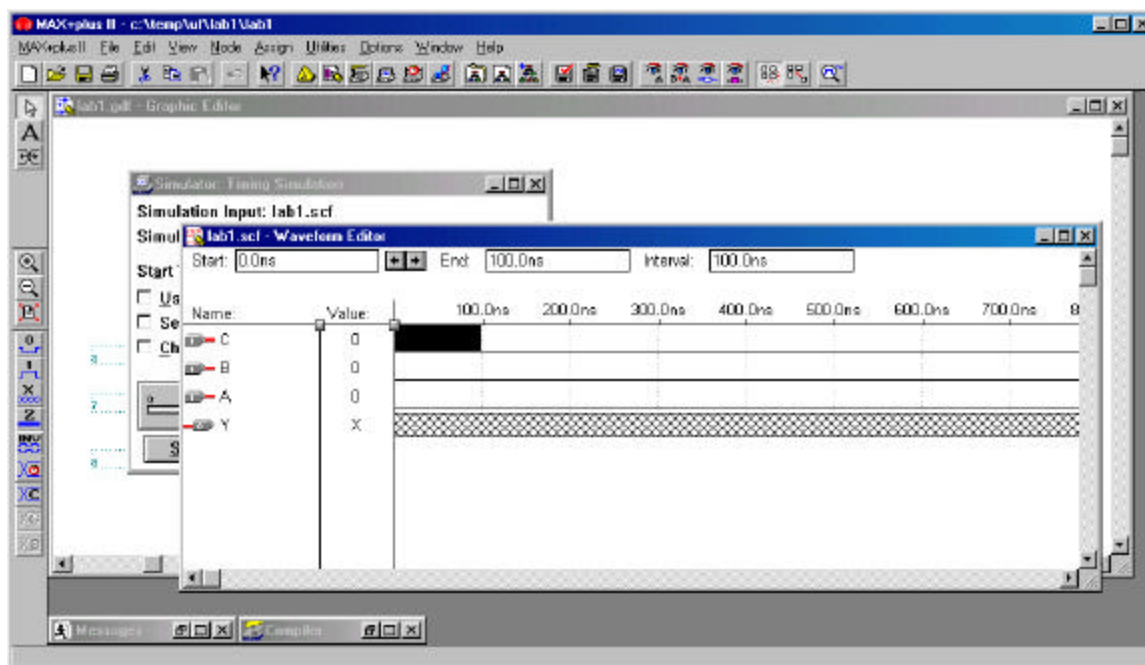


3. Press the start button. You should get an error message that says “Can’t simulate – no scf file loaded for the project”. The simulator is looking for a basic input waveform file (\*.scf) that it can use to excite the circuit fitted into the part.
4. Press the upper pull-down menu button “Max+plus II” and select the “Waveform editor” option. This opens an untitled waveform window.
5. Press the upper pull-down menu button “File” and select “save as”. In the “Save as” window type the file name in ‘lab1.scf’. You have just renamed the untitled waveform window to ‘lab1’ which matches your project name. Thus when you run the simulator, it will automatically use this \*.scf file that matches the lab1 project.
6. Place your mouse inside the ‘lab1.scf – Waveform editor’ window, move it to the area under Name: Value: and right click your mouse. Click on “Enter Nodes from SNF...”. You should see the following window open:

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7. Press the “List” button. You should now see all the inputs & outputs (i.e. A,B,C,Y) for the design listed in the “Available Nodes & Groups” field. Highlight them with your mouse and press the “=>” button. A, B, C and Y should appear in the “Selected Nodes & Groups” field. Press “OK” to move these signals to the waveform editor window and to close this window.
8. The waveform editor window (lab1.scf) now should have inputs A, B, and C as well as output Y in it. Press the (-) magnifying glass on the left most tool bar of the main MaxPlus window. You should now see the following time scale for the waveform editor window:

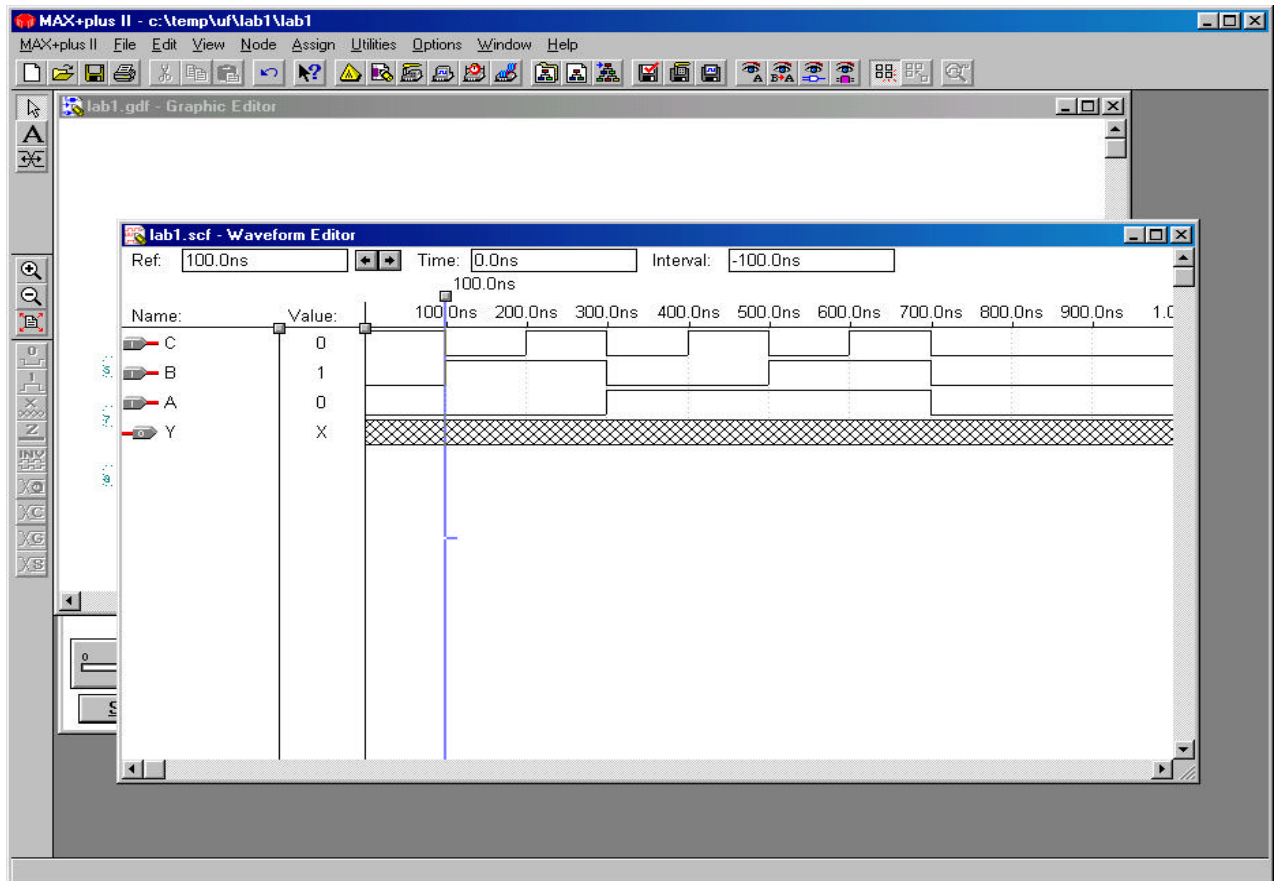




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**Special Note:** The time scale is shown in increments of 100nsec. This is the shortest amount of time that we can set a particular value for a given input. In other words we can set the first 100 nsec segment of input C (shown darkened in the previous window) to either '1' or '0'. However we can not set a smaller segment (i.e. 50 nsec) to '1' or '0' ... we have to work with 100 nsec segments. We will learn how to alter this minimum time segment value later.

- Using your mouse, drag it across the 100 nsec segment that was shown as a darkened area in the last window snapshot. You should see a darkened area as result of this operation. Now press the far left toolbar button that has a "1" in it. Now try pressing the far left toolbar button that has a "0" in it. This is how you set the highlighted input segment to a particular value. Set it to '1' and point & click your mouse to a new area on the window to make the change permanent.
- Use the (-) magnifying glass (left most tool bar) to again increase the number of 100 nsec segments viewed and modify the inputs so that they look like the patterns shown below:

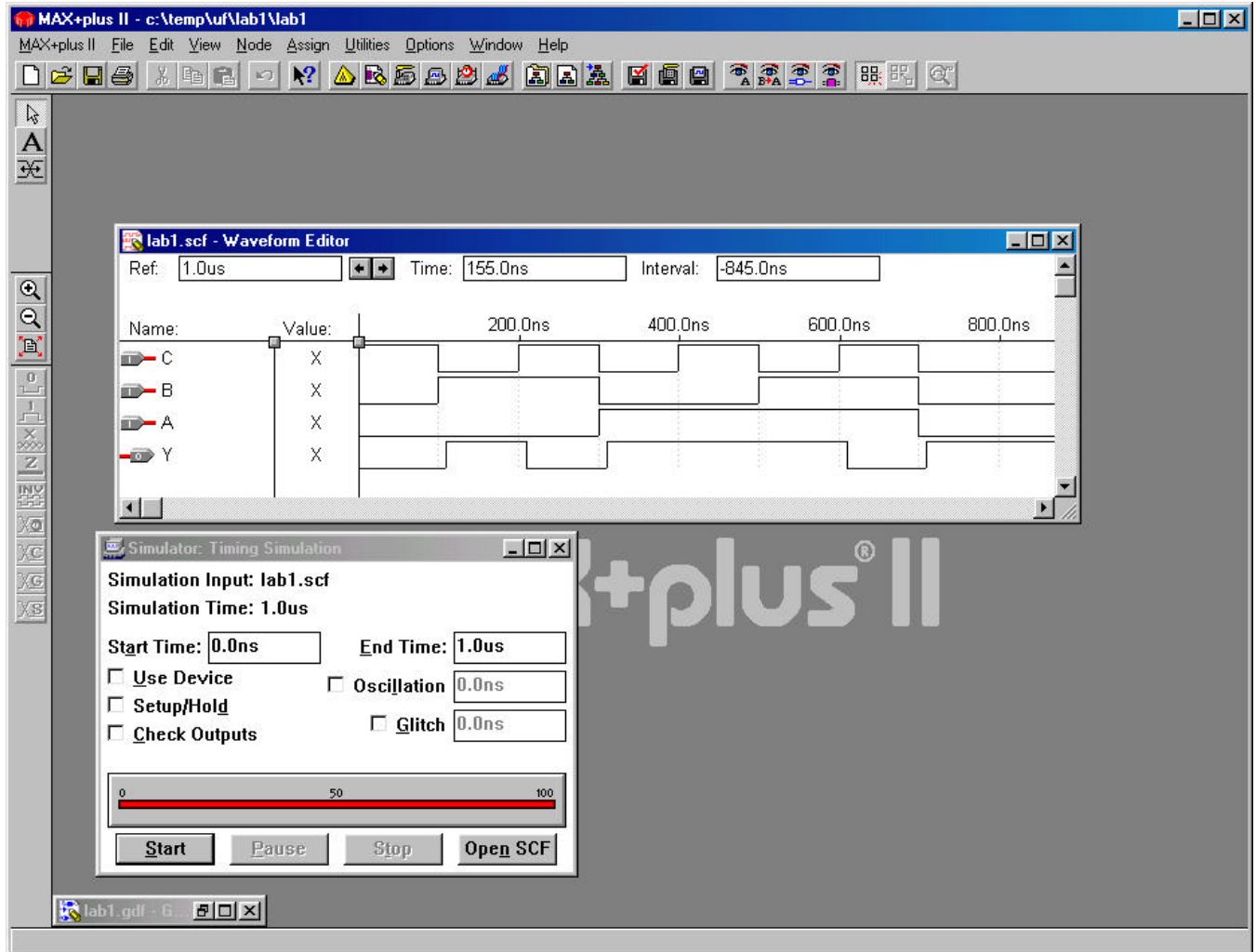


- The inputs have now been defined and 'count' or increment through the binary numbers 001 to 111 (ABC where A is the most significant bit and C is the least significant bit). We can now run the design simulation at this point. Note: The Y output is comprised of 'XXX' in the waveform editor to show that the output is presently undefined. The reason that it is undefined is that although the inputs have been defined, the simulation has not been run yet.

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### C. Running the Simulator and Analyzing the Results

1. To run the simulator, simply press the “Start” button on the Simulator: Timing Simulation Window. You should see a red bar scroll across the bottom of this window and a small ‘project simulation complete’ window should appear. Press “Ok” to get rid of this window.
2. If you haven’t created a logic table for the equation you entered under MAXplus II, do so now and compare these results with those obtained from simulation. Your simulation results from MAXplus should look as follows:



3. When comparing the results of the logic table with that of the simulator, it should be apparent that they match but that there is a small delay between when the inputs change and when the output changes to the expected value. For example, if we look at the time segment from 200 to 300 nsec we see that the inputs C & B are ‘1’ for the interval, A is ‘0’ and the resulting output changes from a ‘1’ to its stable value ‘0’ a short time after the 200 nsec mark. This slight delay is due to the physical gate delay of the gates in the CPLD required to implement the inverter/and/or circuit. In other words, every gate in your circuit has a chunk of FPGA hardware that is associated with it and an associated physical delay. With this new knowledge, what do you think is the worst delay path in your circuit?