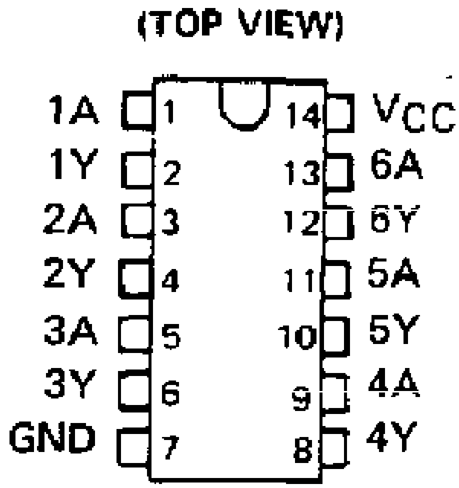
2 A Simple Logic Gate

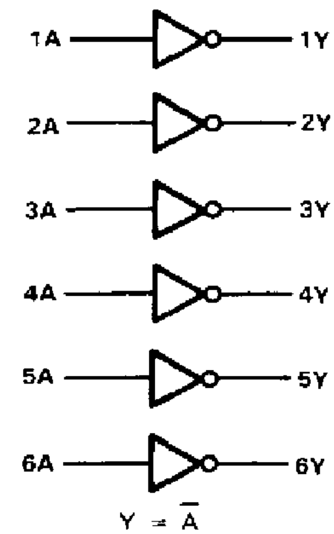
- This experiment introduces the student to a simple logic element, an **inverter**, contained in a 14 Dual-in-line (DIP) package. The student will use equipment skills learned in the first lab to measure the **propagation delay** of the inverter.

I. 7404 Logic Gate

Appendix I contains the datasheet for a 7404 logic gate. Datasheets for 74XX family devices can be found on the WWW at the Texas Instruments data sheet web site:
http://www.ti.com/sc/docs/products/logic/index.htm

Datasheets can also be found in your TTL logic databook. Below is the pinout for the 7404 (in future labs, you will be expected to look up the datasheet yourself on the WWW or in your databook and have the datasheets with you in lab).





The VCC pin should be connected to +5 V for this part, GND is connected to the COM terminal on the test box. Note that pin #1 is to the left of the “notch” located at one end of IC; the notch is used to locate pin #1.

A. With the testbox OFF, connect a 7404 IC chip as follows.

1. +5V to pin #14
2. GND to pin #7
3. Data Switch 1 (DS-1) to pin #1
4. Data Indicator 1 (DI-1) to pin #2

B. After your instructor checks your circuit, turn the breadboard on.

C. Observe the LED output and measure both the input and the output voltages using the digital multimeter with the data switch in both positions (record measurements on datasheet at end of lab). Repeat these measurements after connecting in parallel the five remaining inverters to the output of the first (this checks to see if one inverter output can drive the inputs of 5 inverters simultaneously).

D. Using techniques learned from Lab #1, display the INPUT of the inverter (pin #1) on Oscilloscope channel #1 and the OUTPUT of the same inverter (pin #2) on Oscilloscope channel #2. Connect the input of the inverter to the 1 Mhz digital clock output on the test box. Display both Channels (#1, #2) simultaneously on the scope.

E. Observe the two waveforms on the oscilloscope. Channel 1 is showing the input to the logic gate, an inverter. Channel 2 is showing the output of the inverter.

F. With the digital clock output set at 1 MHz use the 7404 output pin 2 to drive the remaining five inverters connected in series as shown in Figure 2.1. Because there is an even number of inverters in this chain, a rising edge on the input of the first inverter will be a rising edge on the output of the 2^{nd} inverter. The output waveform is DELAYED by the sum of the propagation delays through the 6 inverters (see Appendix I for a definition of propagation delay). Use the oscilloscope and the techniques learned in Lab #1 to measure the time difference between rising/falling edges on the input of the first inverter to rising/falling edges on the output of the last inverter. By measuring the propagation delay through the five gates with respect to positive and negative edges of the clock at pin 1, calculate the average 7404 t_{PHL} and t_{PLH} delay.

G. Repeat the previous delay measure except use rising/falling edges at pin #2 to falling/rising edges at pin #12.

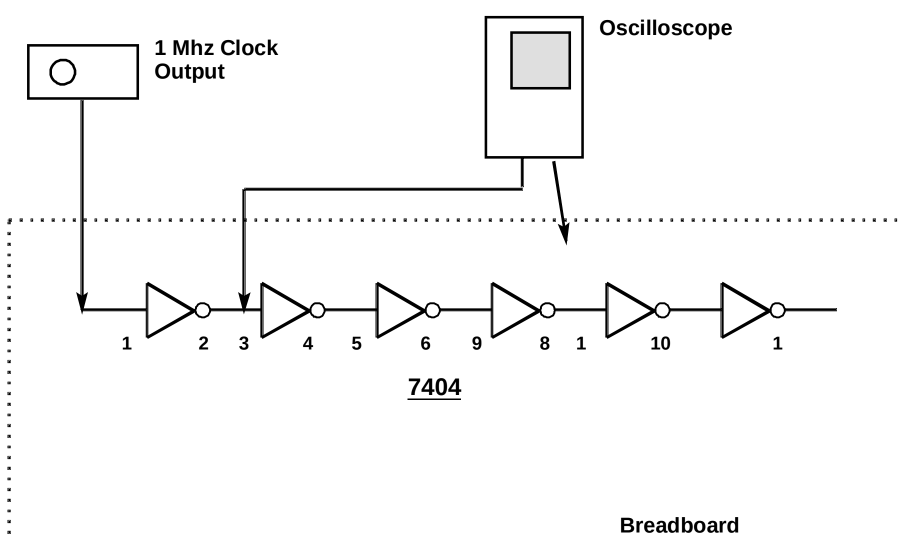


Figure 2.1

II. Lab Data Sheet

(A) TA CHECK OFF SIGNATURE: ________________

Single logic **INVERTER**

	Input (V)	Logic Input	Output (V)	Logic Output
"Up"				
"Down"				

One **INVERTER** driving 5 inverters:

	Input (V)	Logic Input	Output (V)	Logic Output
"Up"				
"Down"				

(F) Six Inverters, Sketch the input and output waveforms (Label TPHL, TPLH propagation delays on sketch!!)

Measured TPHL propagation delay thru 6 inverters: ____________ Average Delay: ___________

Measured TPLH propagation delay thru 6 inverters: ____________ Average Delay: ___________

(G) Five INVERTERS

Measured TPHL propagation delay thru 5 inverters: ____________ Average Delay: ___________

Measured TPLH propagation delay thru 5 inverters: ____________ Average Delay: ___________

LOCATE the propagation delay given in the DATA SHEET for the 7404 and COMPARE THIS VALUE to the values above.
Comments on 7404 data sheet propagation delay and measured average delay:

Formulas:

$$\text{Propagation delay, } t_{pxx} = \frac{\Delta t}{M * G} \quad \text{seconds}$$

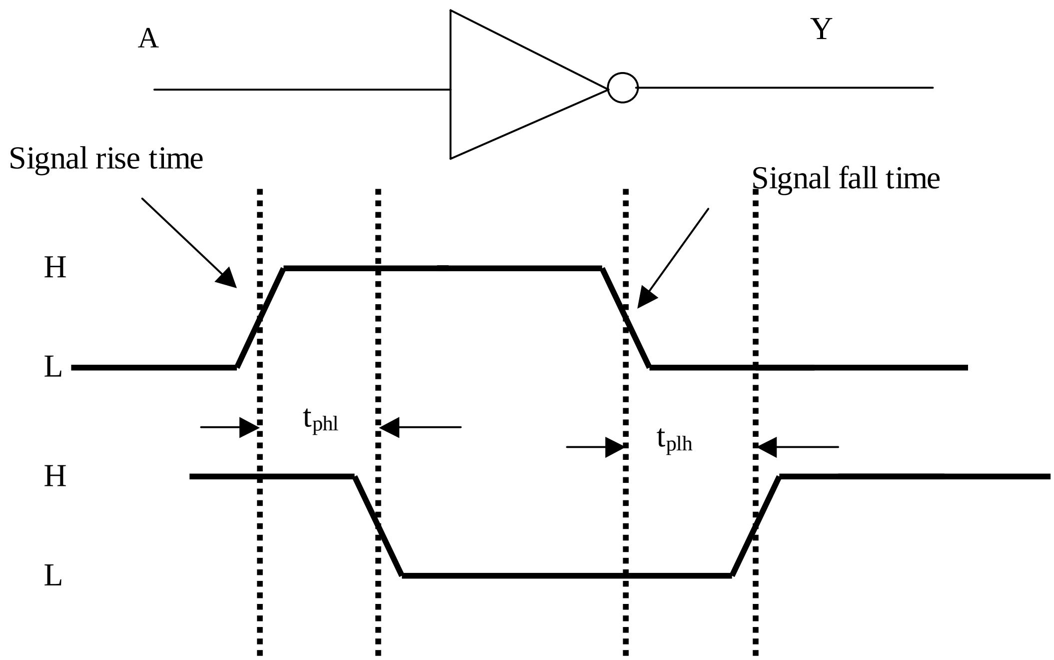
Δt = Time difference between CH1 and CH2.
M = multiplier used on the oscilloscope (will usually be 1 or 10)
G = number of logic gates used.

$$Frequency = \frac{1}{Period}$$

Appendix I: Propagation Delay

Propagation delay is the delay from a change on an input to a change on the output. TPHL is the propagation delay for an input change causing a HIGH to LOW change on the output (this does NOT REFER to input change). TPLH is the propagation delay for an input change causing a LOW to HIGH change on the output.
The figures below define TPHL, TPLH for inverting and non-inverting gates.

Propagation Delay (inverting)



Propagation Delay (non inverting)